Welcome To

ISSCC 2014
Session 29
Data Converters for Wireless Systems

A 5mW CT ΔΣ ADC with Embedded 2nd-Order Active Filter and VGA Achieving 82dB DR in 2MHz BW

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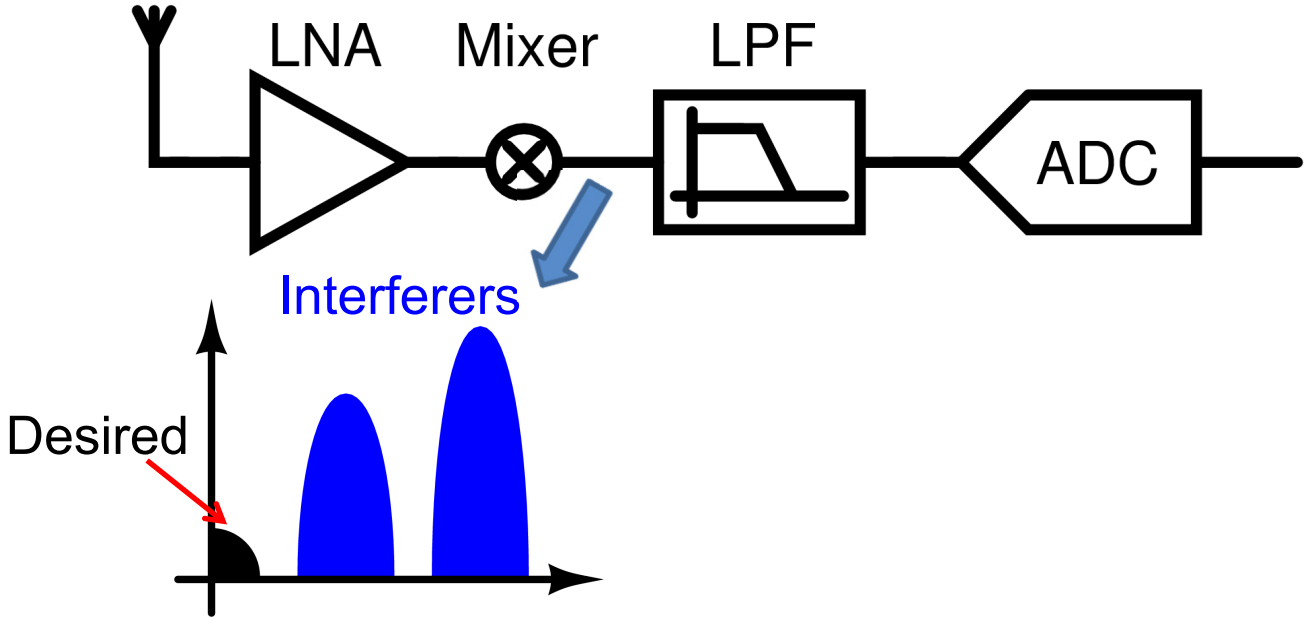
Outline

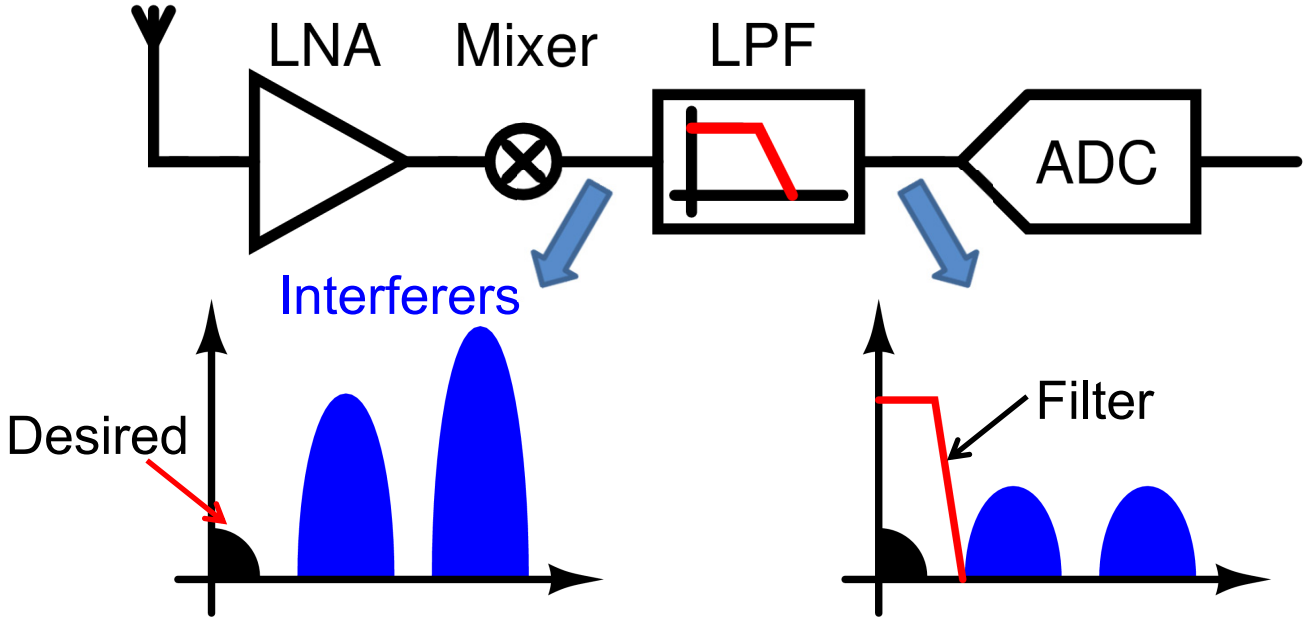
- Motivation
- Embedding a filter in a CTDSM
- Modulator prototypes
  - Upfront filter
  - Embedded filter
- Measurement results
- Conclusions

Motivation

Wireless receivers



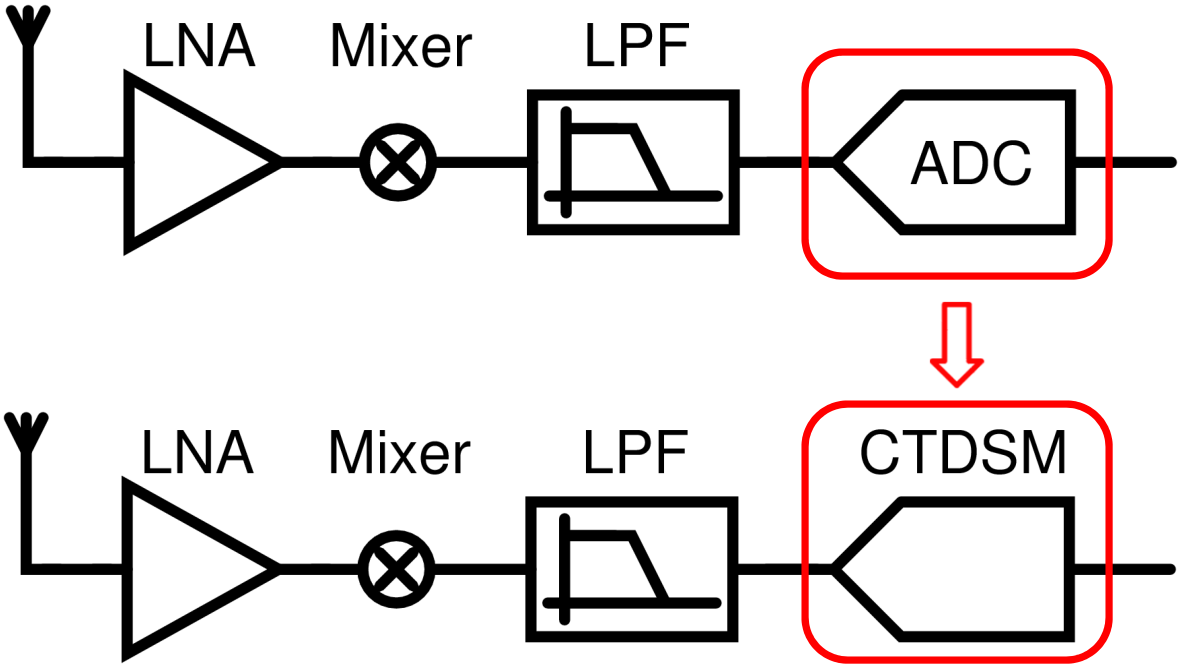
Wireless receivers



LPF

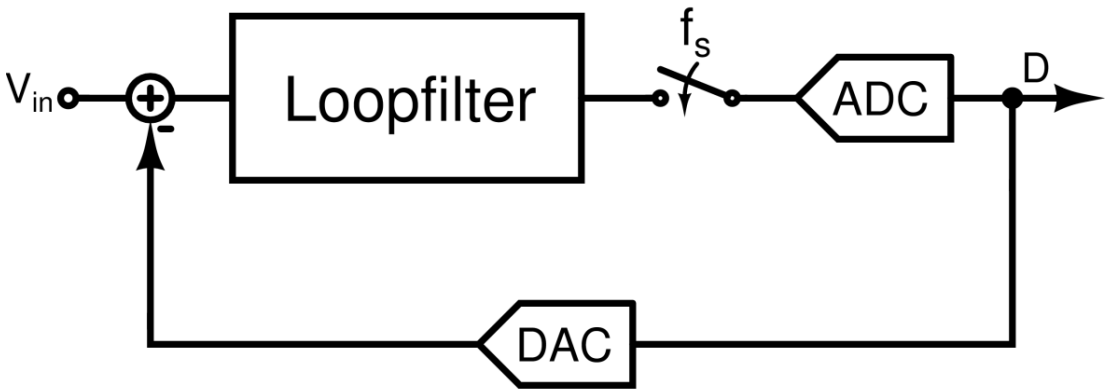
- Antialiasing
- Interferer rejection
  - Reduces DR requirement on ADC

Continuous-time ΔΣ modulators



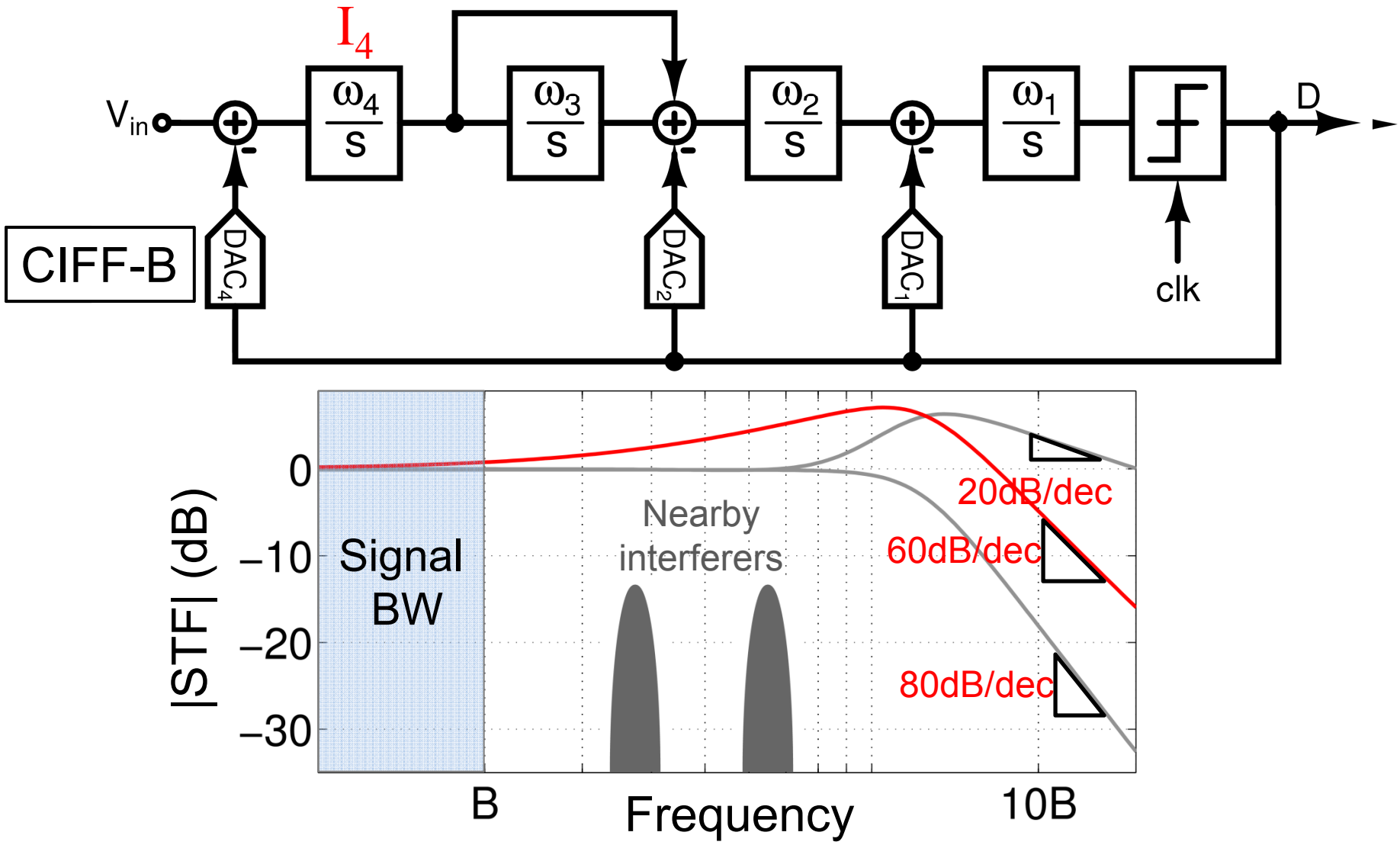
- Continuous-time ΔΣ modulators (CTDSMs) :
  - Implicit antialiasing
  - Filter needed to attenuate interferers

STF of a CTDSM



- STF depends on loop filter topology
- Bandwidth of STF
  - Depends on NTF
  - Cannot be controlled independently

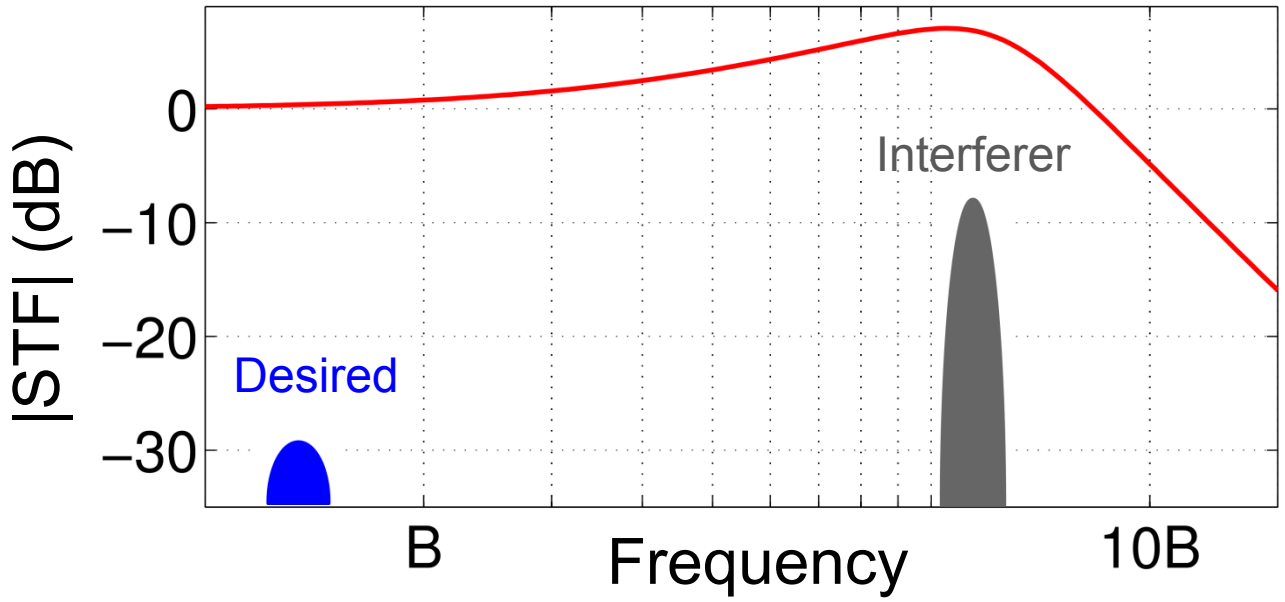
STF : CIFF-B loop filter



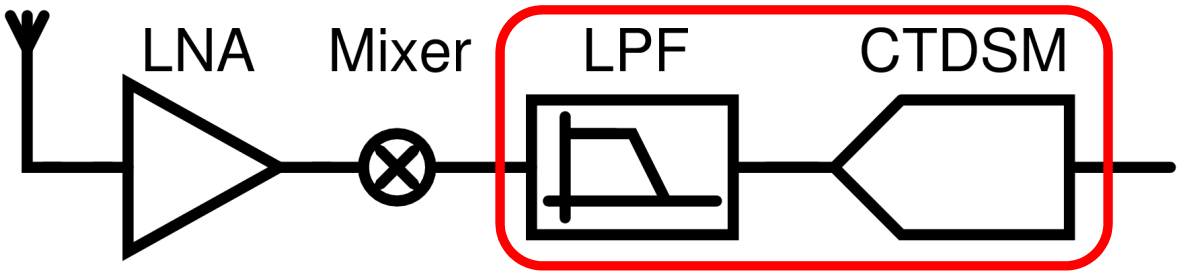
With interferers

- STF peaking reduces max. input amplitude
- Needs lower in-band noise for same SNR

  →Increases power consumption



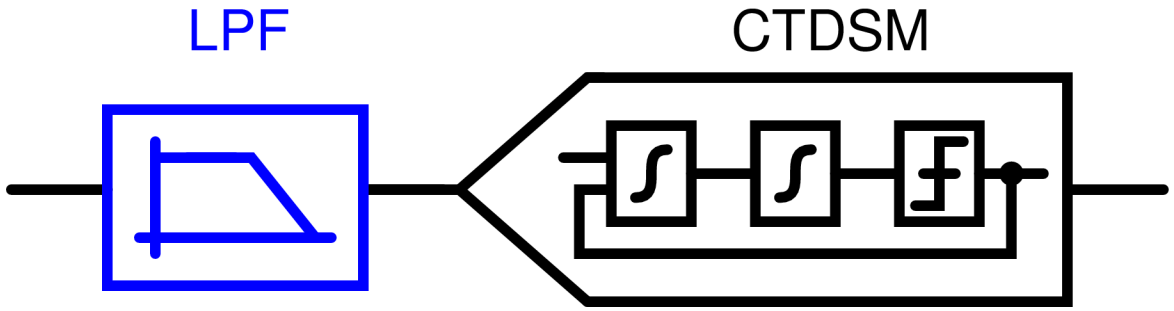
Filter + CTDSM



- LPF modifies STF & attenuates interferers
  - Better than standalone modulator

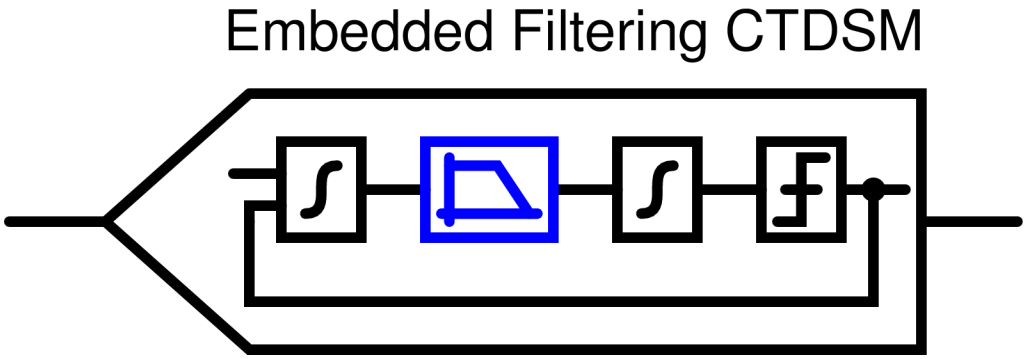
Filter + CTDSM

H_1-ΔΣ



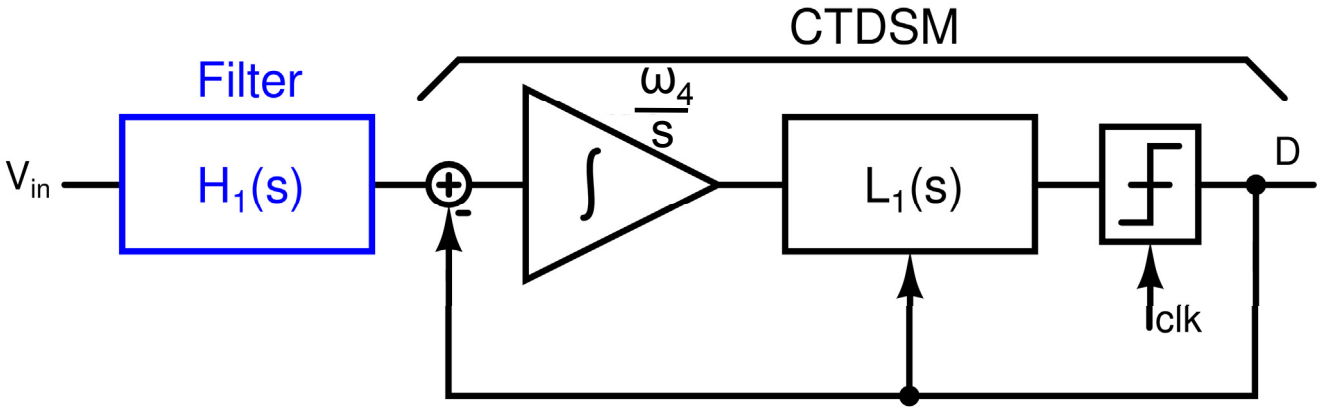
- Filter adds noise and distortion
- This work moves filter into the modulator
  - Reduces noise and distortion for same power

Δ-H_1-Σ

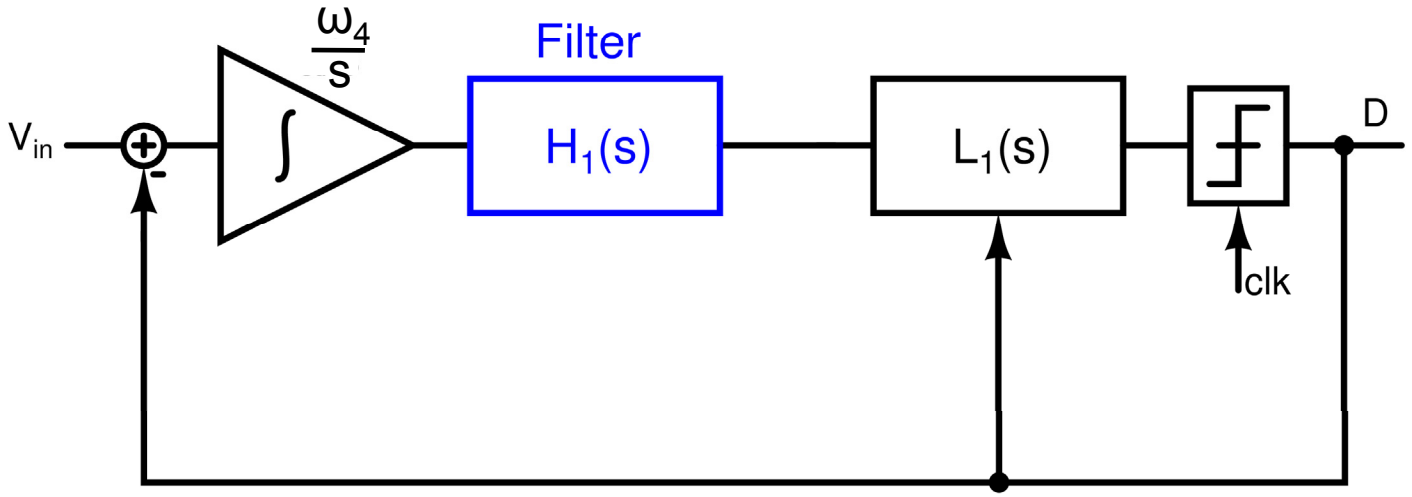


Basic idea & prior art

Upfront filtering (H_1-ΔΣ)

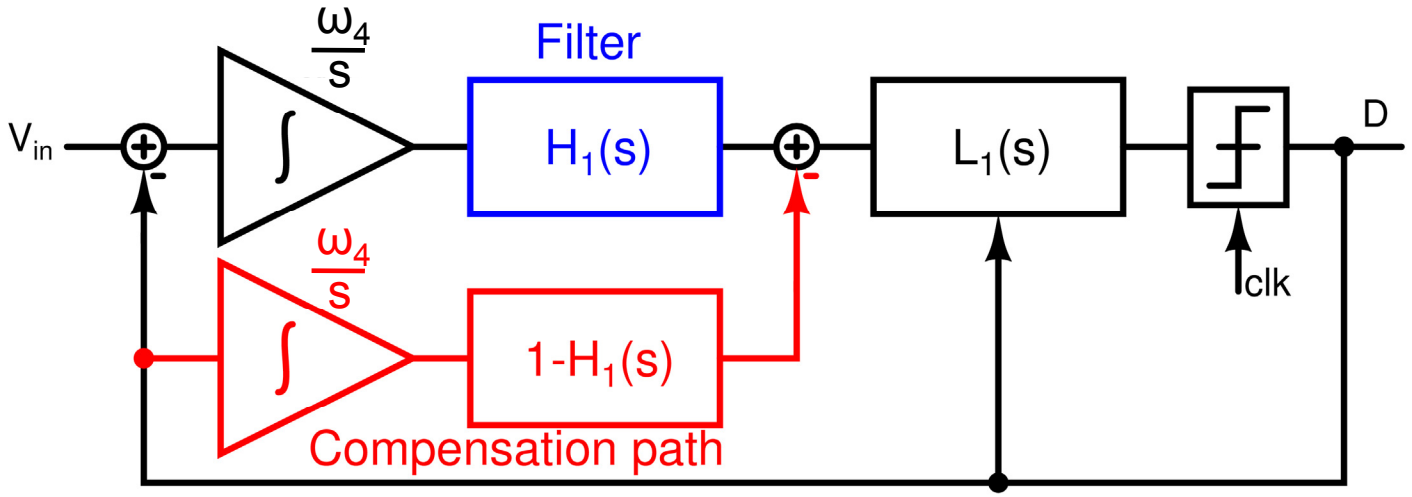


Embedded filter (Δ-H_1-Σ)



- Noise from H_1 – divided by gain of 1st integrator
- $H_1(s)$ affects loop stability

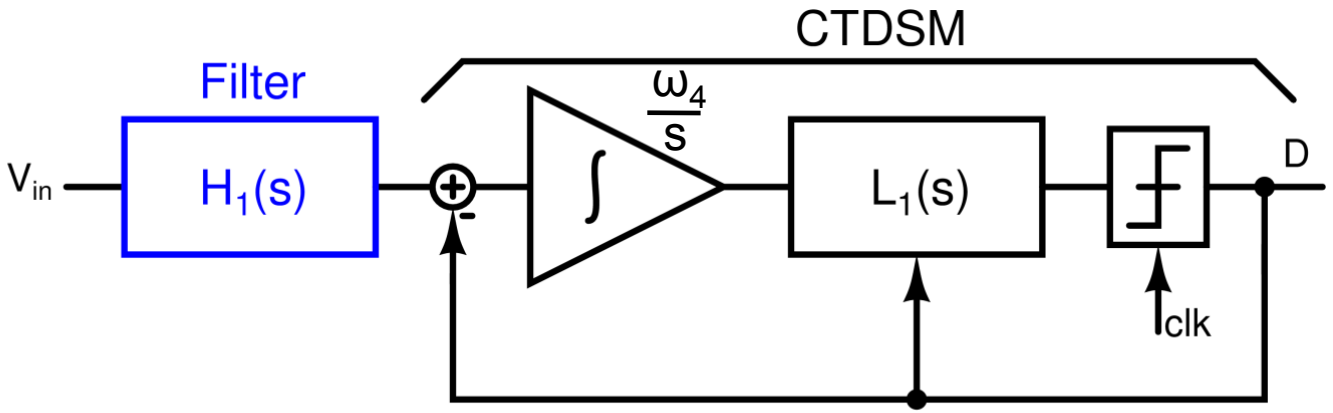
Embedded filter (Δ-H_1-Σ)



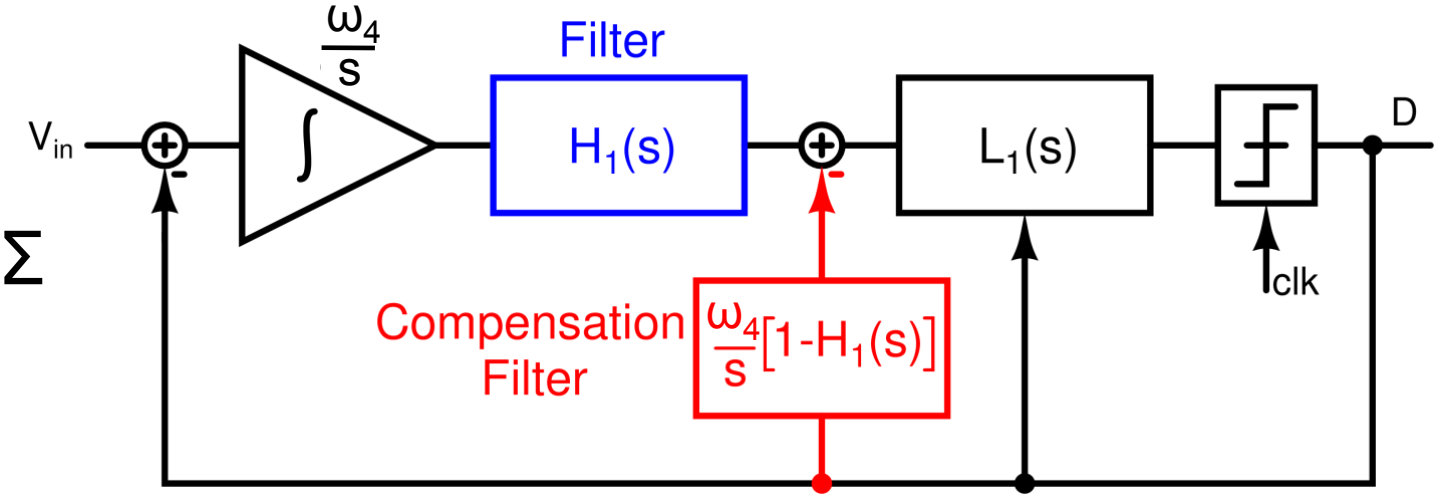
- Loop stabilized by adding $\frac{\omega_4}{s}[1-H_1(s)]$

H_1-ΔΣ and Δ-H_1-Σ

H_1-ΔΣ

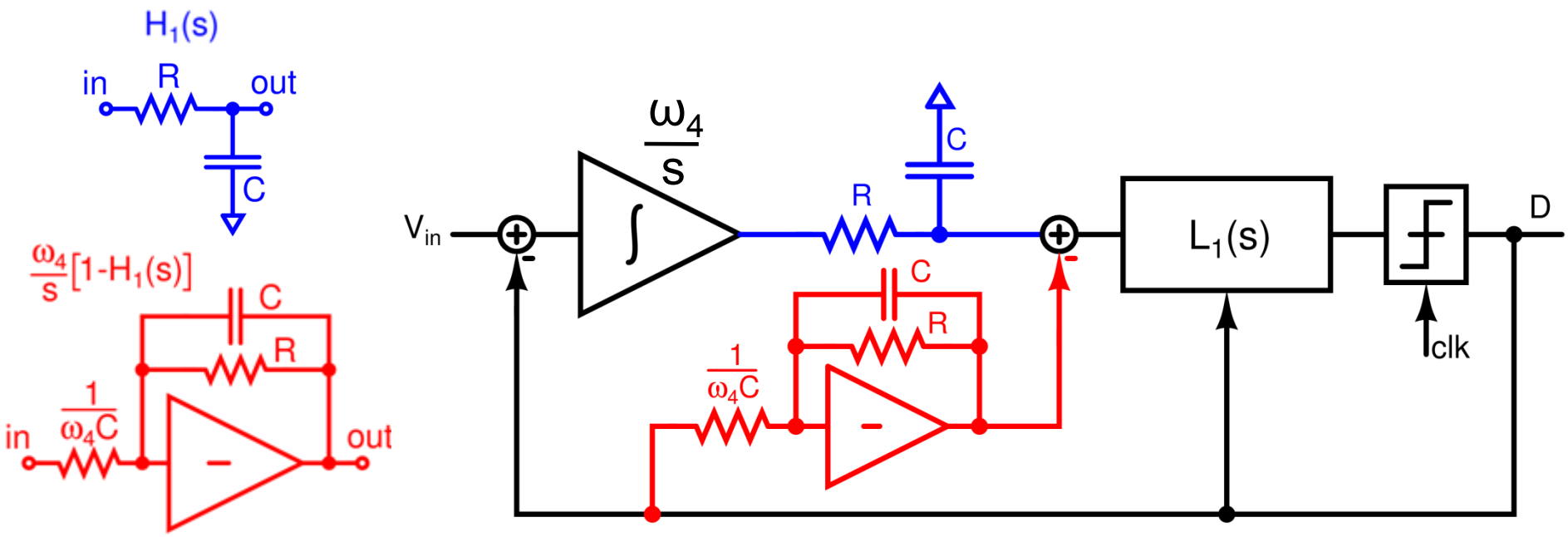


Δ-H_1-Σ



- STF and NTF of both modulators are equal

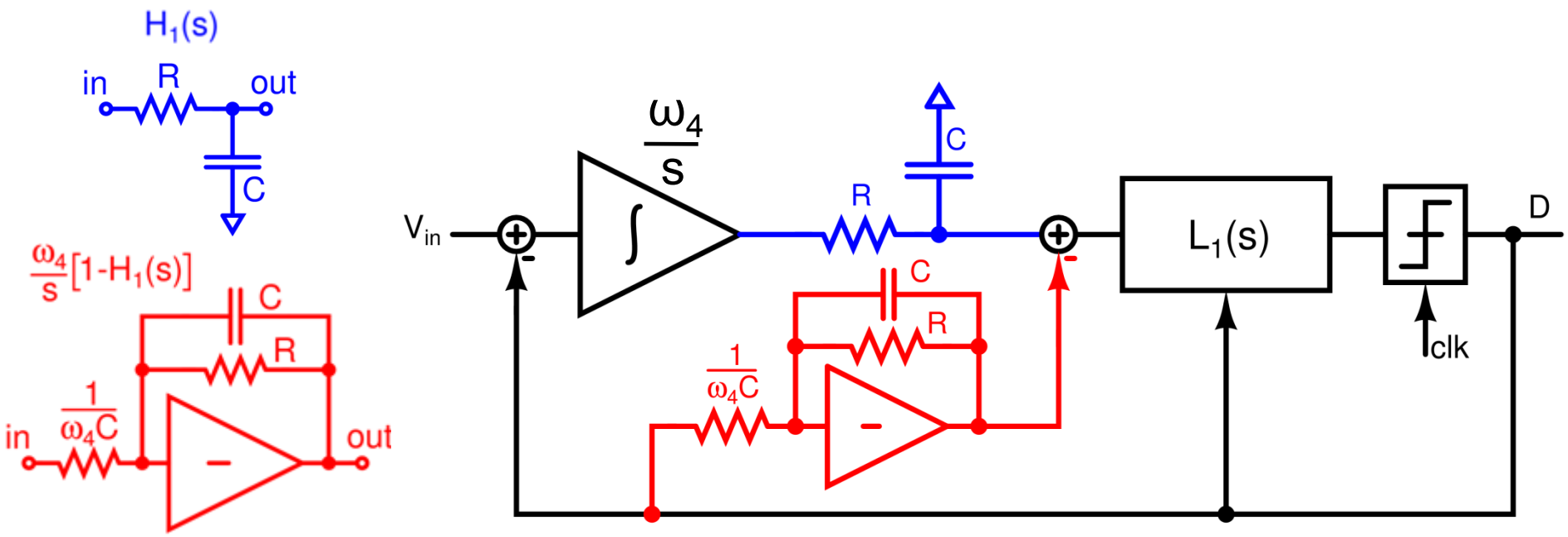
Prior art



- $H_1(s)$: 1st order RC filter
- Active compensation filter
- 1 bit DAC

K. Phillips, et. al, "A 2mW 89dB DR Continuous-time ΔΣ ADC with increased immunity to interferers," *Proc. of the ISSCC, Feb. 2004*

Prior art

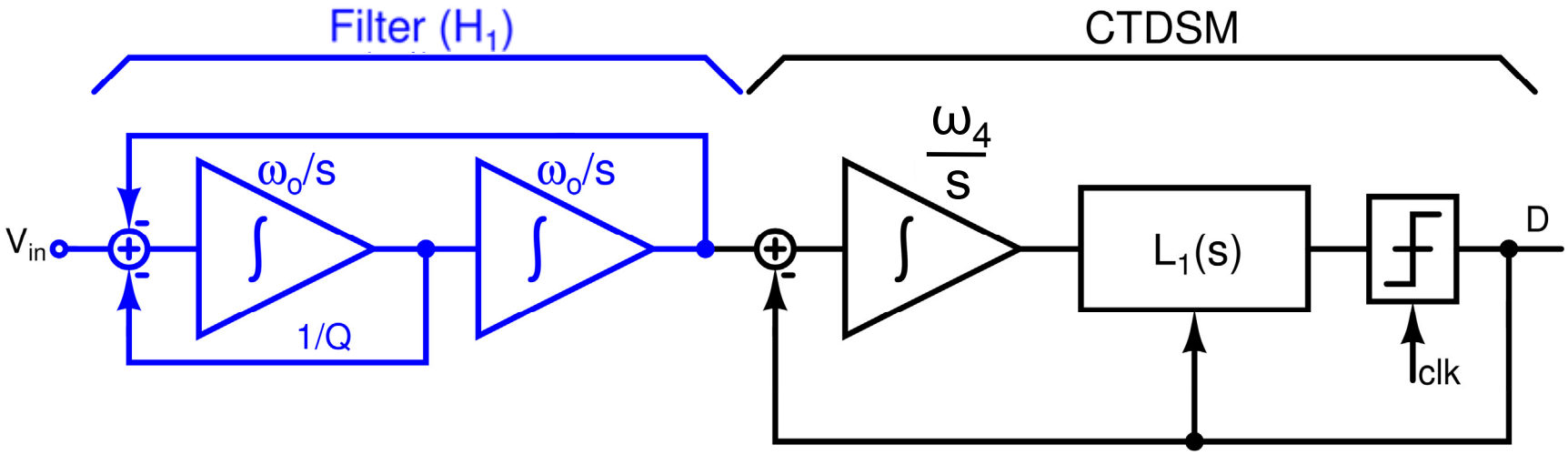


- $H_1(s)$: 1st order RC filter → limited selectivity
- Active compensation filter → extra opamp
- 1 bit DAC → jitter and 1st integrator linearity

K. Phillips, et. al, "A 2mW 89dB DR Continuous-time ΔΣ ADC with increased immunity to interferers," *Proc. of the ISSCC, Feb. 2004*

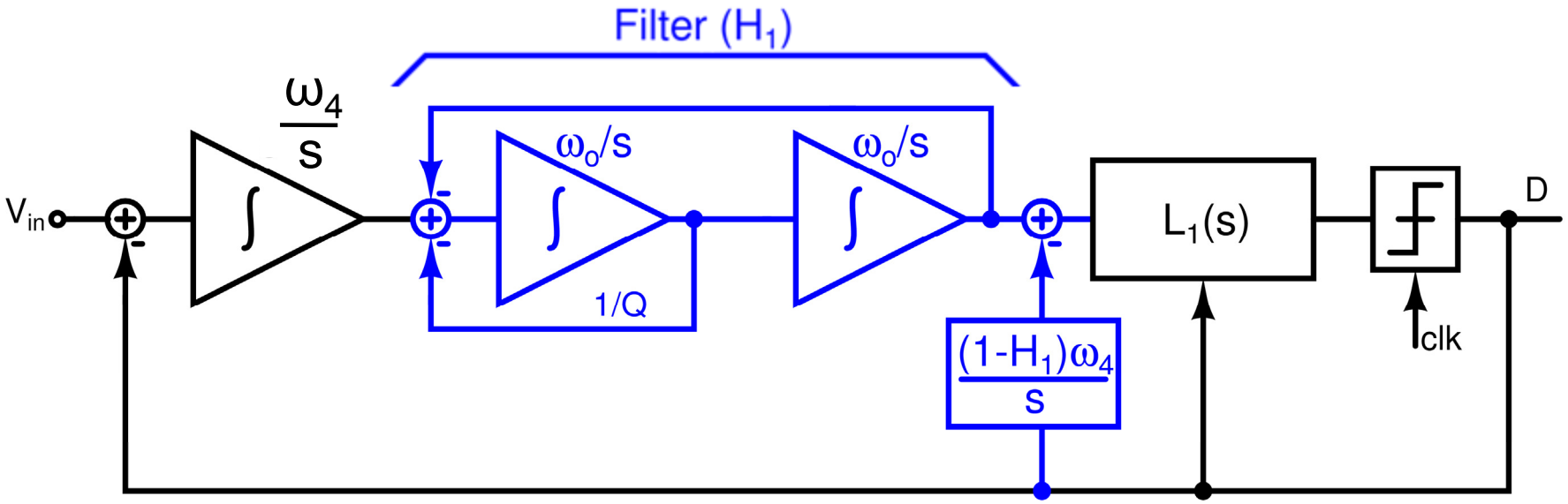
Proposed technique

Filter Upfront (H_1-ΔΣ)



- 2nd order filter (H_1) used before CTDSM
  - Improves interferer rejection

Embedding filter in CTDSM



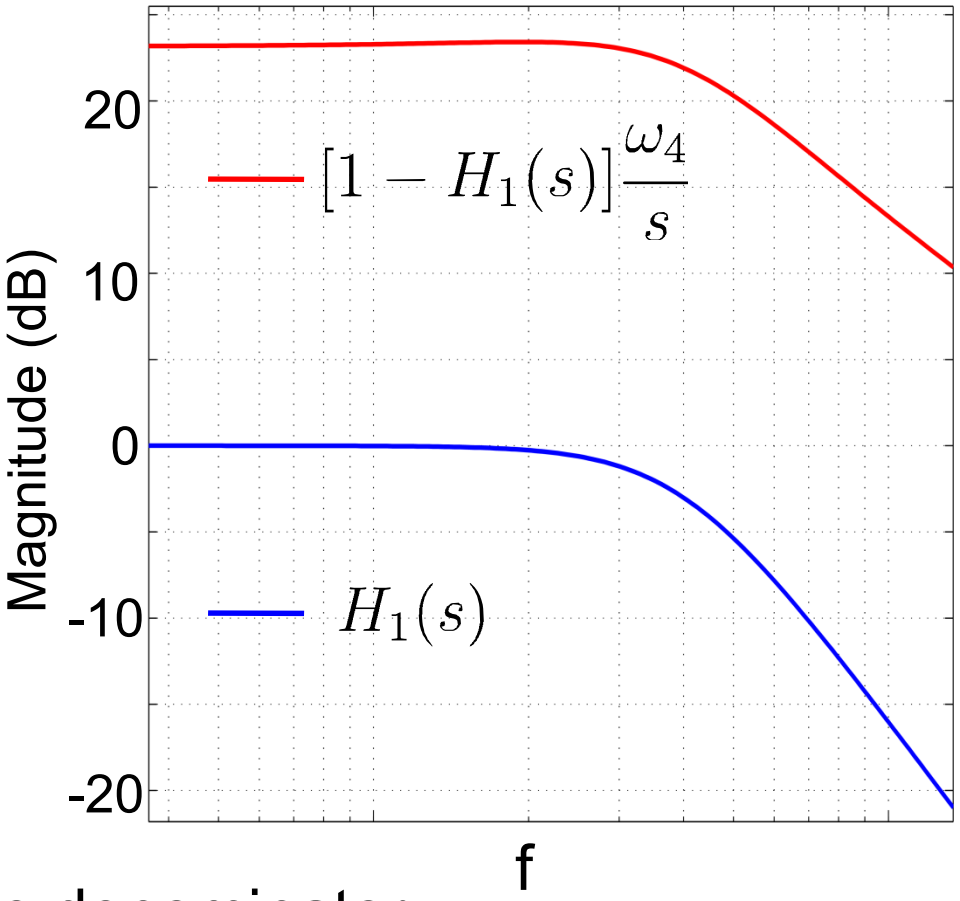
- H_1 moved beyond the 1st integrator
  - Compensation filter needed for loop stability

Filter and compensation filter

$$H_1(s) = \frac{1}{1 + \frac{s}{\omega_o Q} + \frac{s^2}{\omega_o^2}}$$

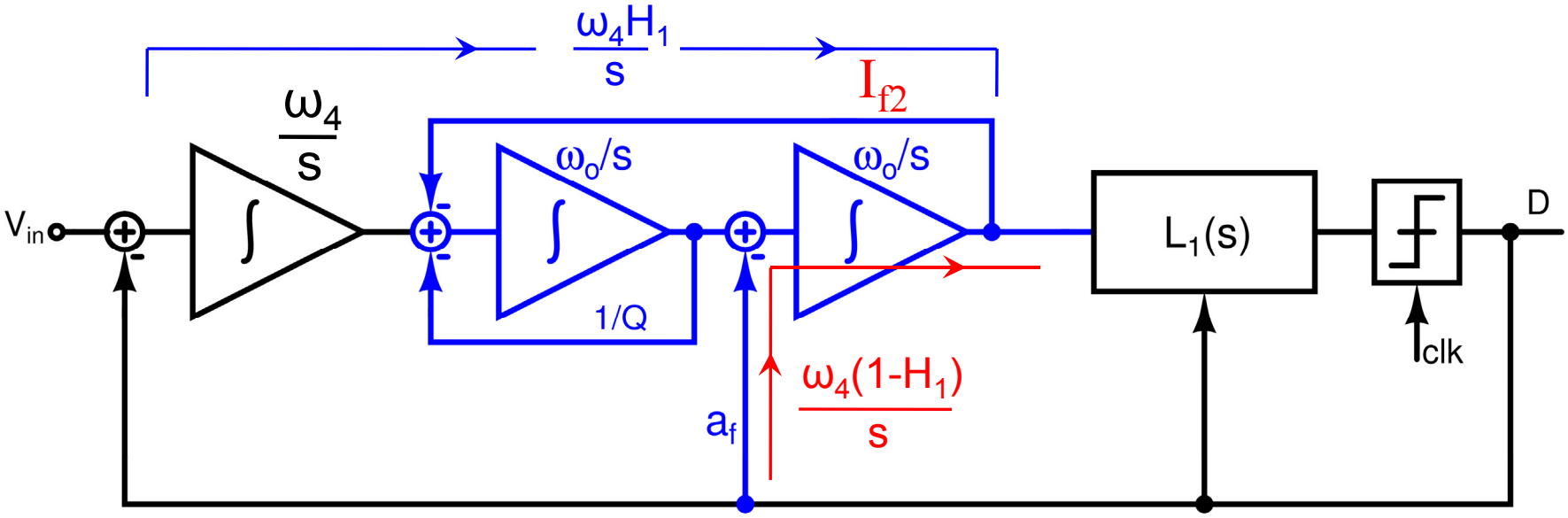
- Comp. filter : $[1 - H_1(s)]\frac{\omega_4}{s}$
- $[1 - H_1(s)]$ has a zero at DC
- Cancels the DC pole

$$[1 - H_1(s)]\frac{\omega_4}{s} = \frac{\frac{\omega_4}{\omega_o Q} + \frac{\omega_4 s}{\omega_o^2}}{1 + \frac{s}{\omega_o Q} + \frac{s^2}{\omega_o^2}}$$



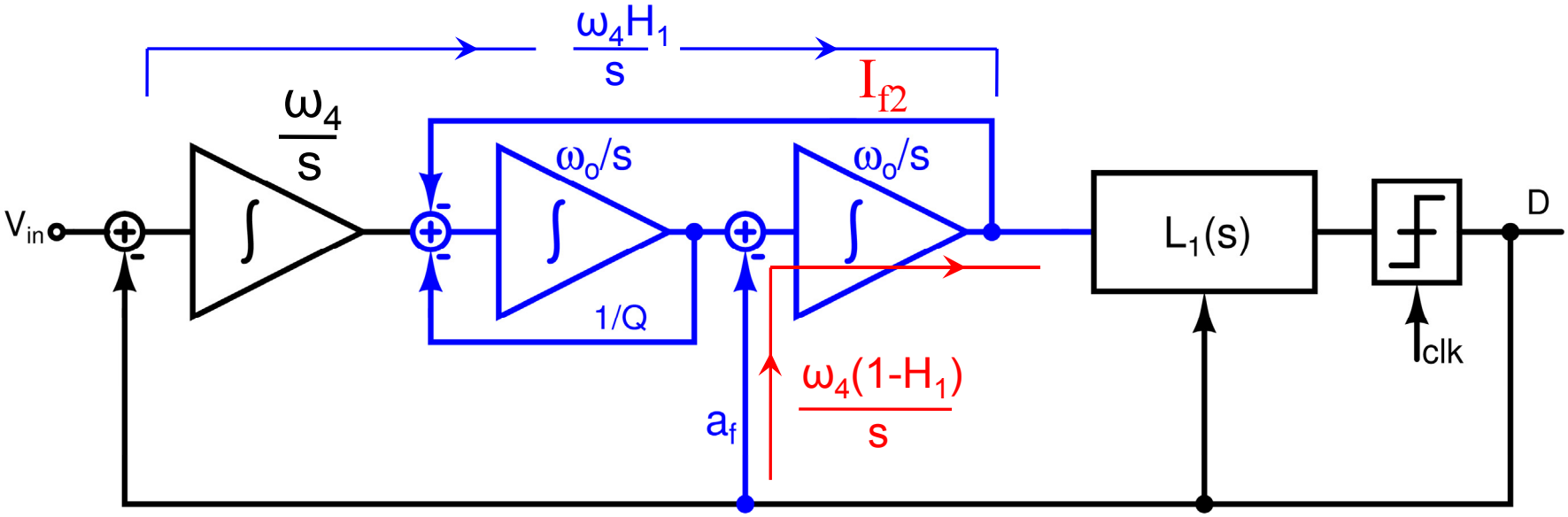
- $H_1(s), [1 - H_1(s)]\frac{\omega_4}{s}$ have same denominator
- Realized using the same filter

Embedding filter in CTDSM (Δ-H_1-Σ)



- Compensation filter
  - Inject modulator output at input of I_{f2}

Embedding filter in CTDSM (Δ-H_1-Σ)

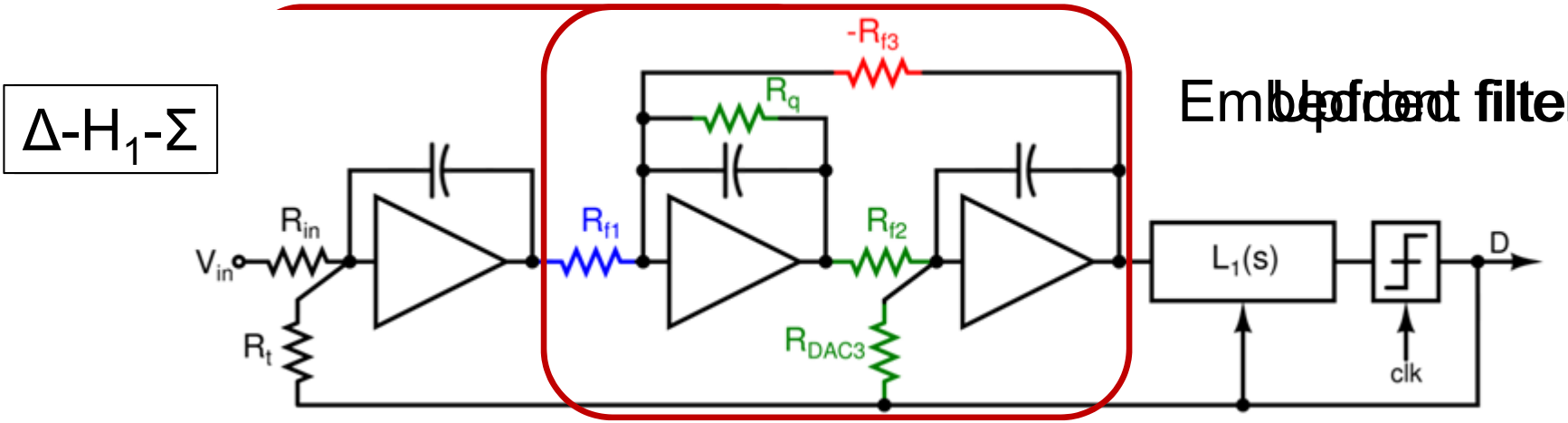


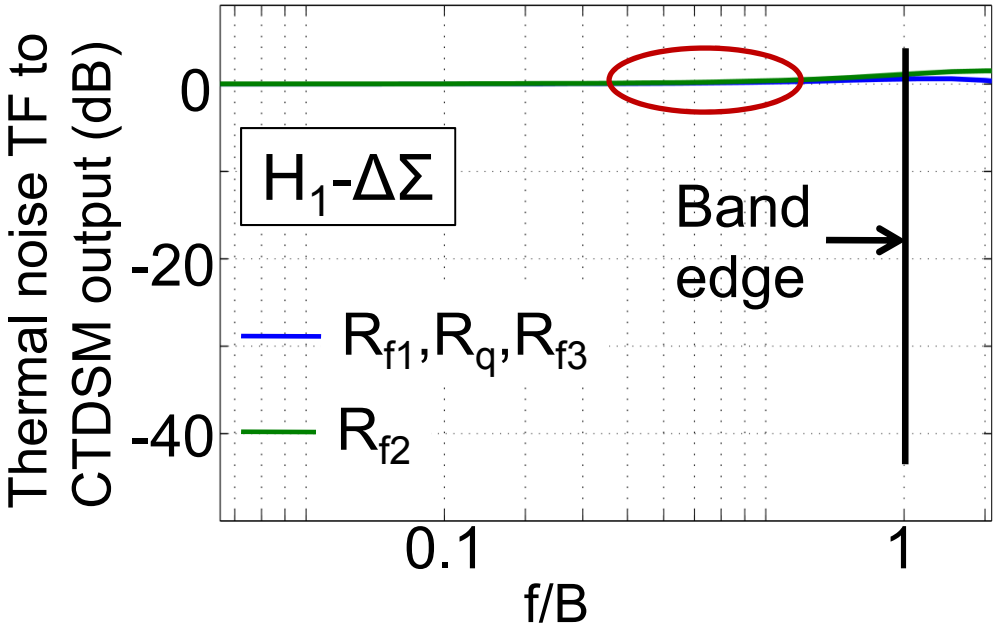
- No extra hardware required
- Can be extended to any filter order
  - Cascade of biquads

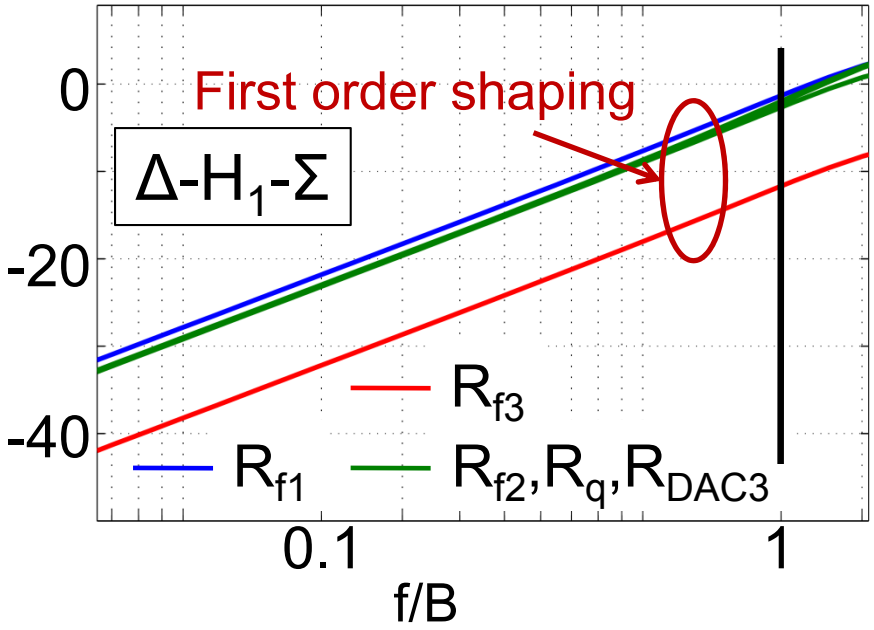
Upfront vs. embedded filtering

- STF and NTF are identical
  - Same functionality
- Performance metrics
  - Noise
  - Linearity
  - Power consumption
  - Area

Filter noise contribution

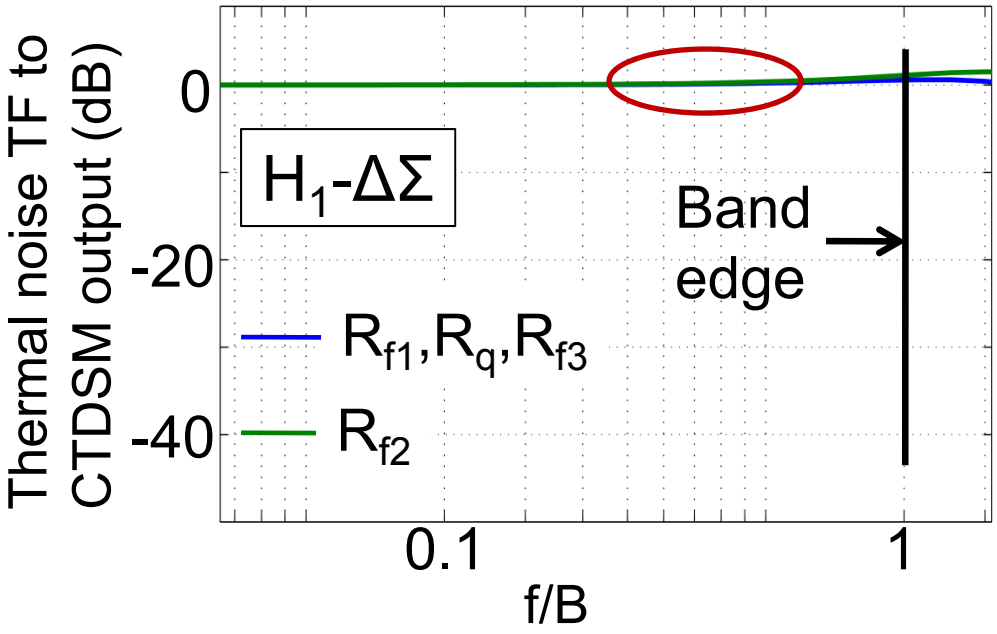


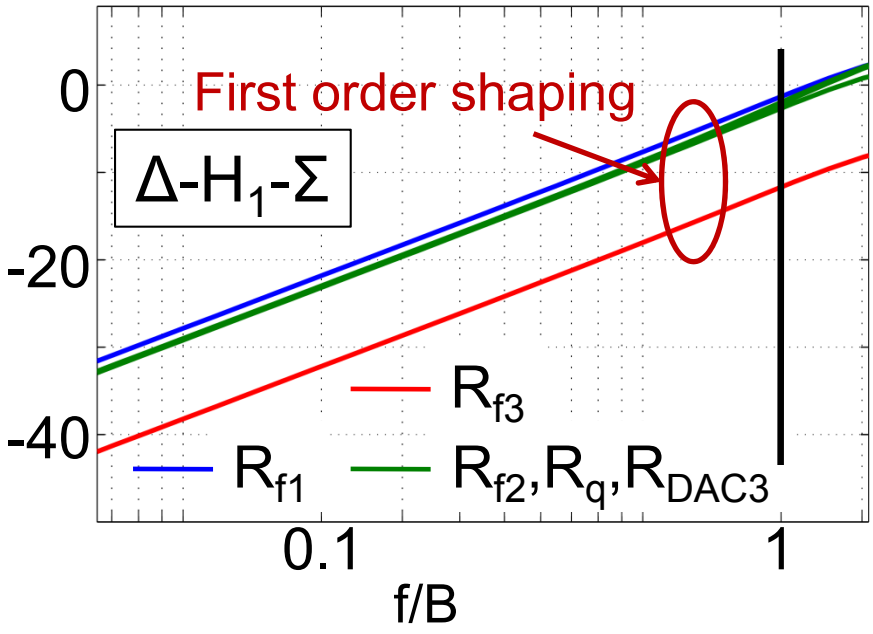




Filter noise contribution

- Δ-H_1-Σ has lesser inband noise





Impedance scaling

- Δ-H_1-Σ can be impedance scaled
  - Same input referred noise as H_1- $\Delta\Sigma$
  - Power consumption reduces
  - Capacitance area reduces

Linearity improvement of Δ-H_1-Σ

- Not changed by impedance scaling
- ≈ same as H_1-$\Delta\Sigma$ for out-of-band frequencies

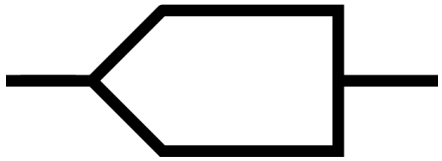
- Power saved (impedance scaling) can be used
  - To increase opamp G_m and improve linearity

Modulator prototypes (0.13μm)

- Upfront filter (H_1-ΔΣ)
- Embedded filter (Δ-H_1-Σ)

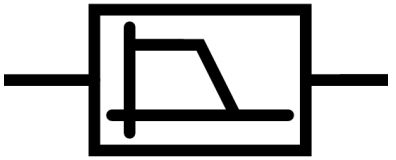
Specifications

CTDSM



- BW = 2 MHz
- OSR = 64
- Order = 4
- NTF OBG = 1.5

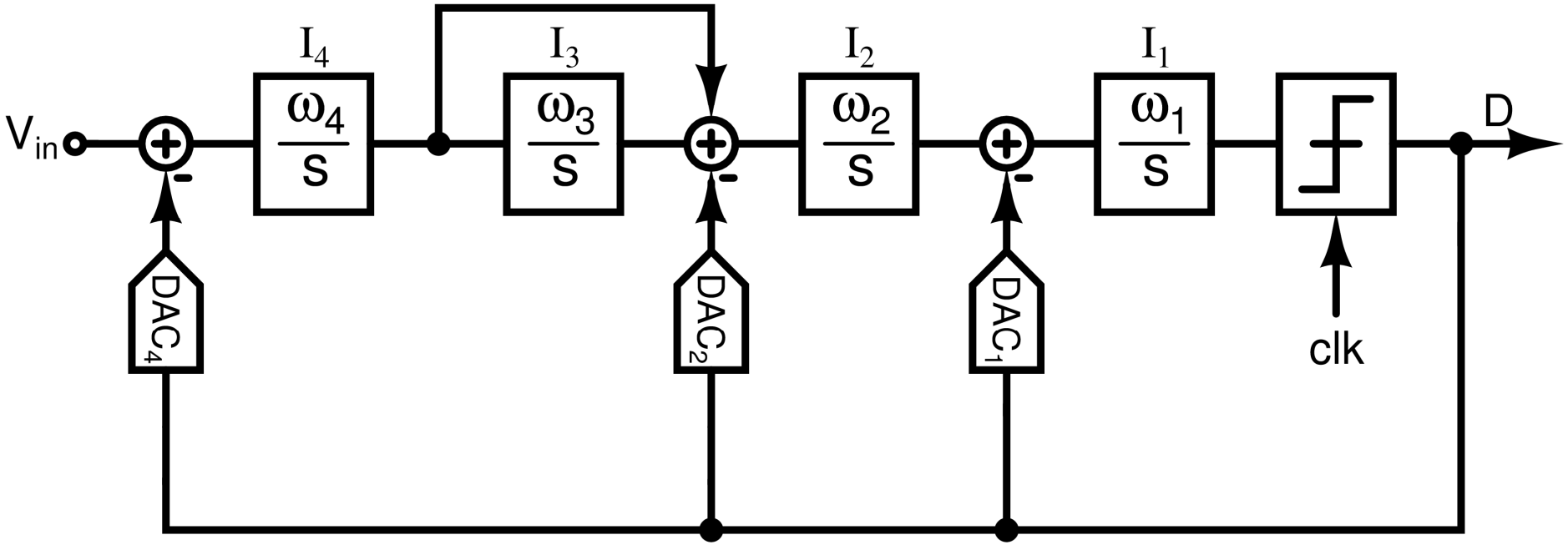
LPF



- Order = 2
- Butterworth
- f_{3dB} = 4 MHz

- VGA : 0 to 18 dB gain
- Input referred DR = 90 dB

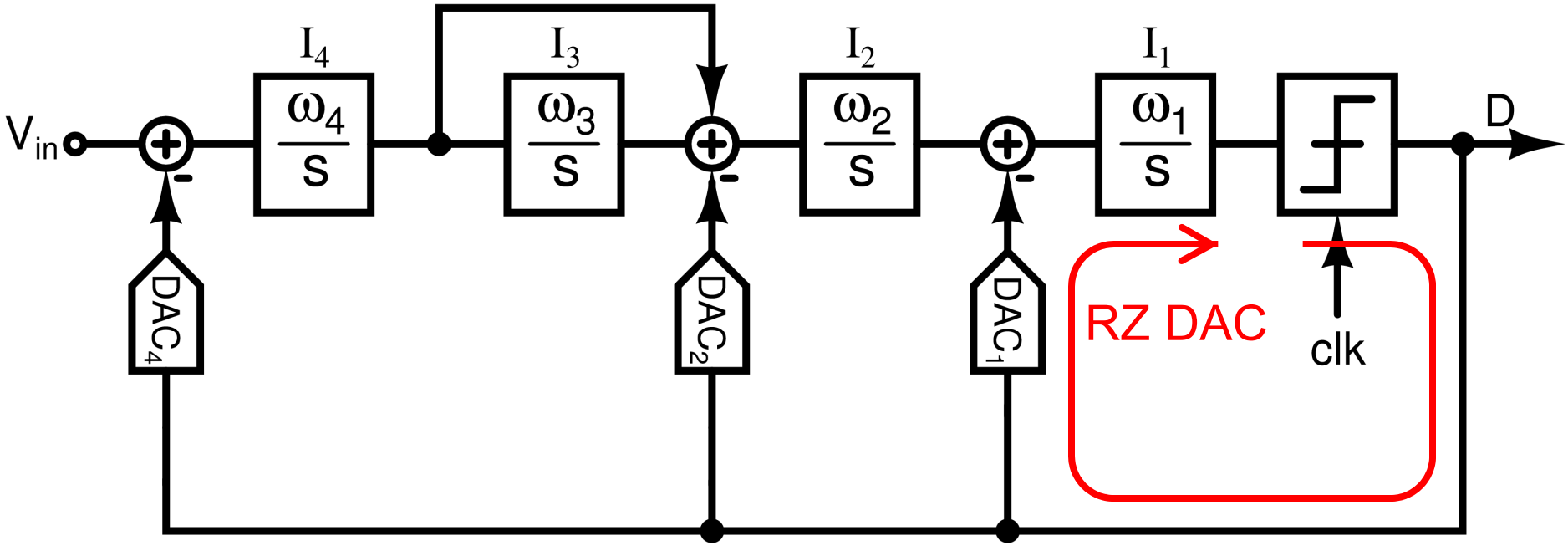
CTDSM architecture



- 4th order single bit modulator
- CIFF-B loop filter topology

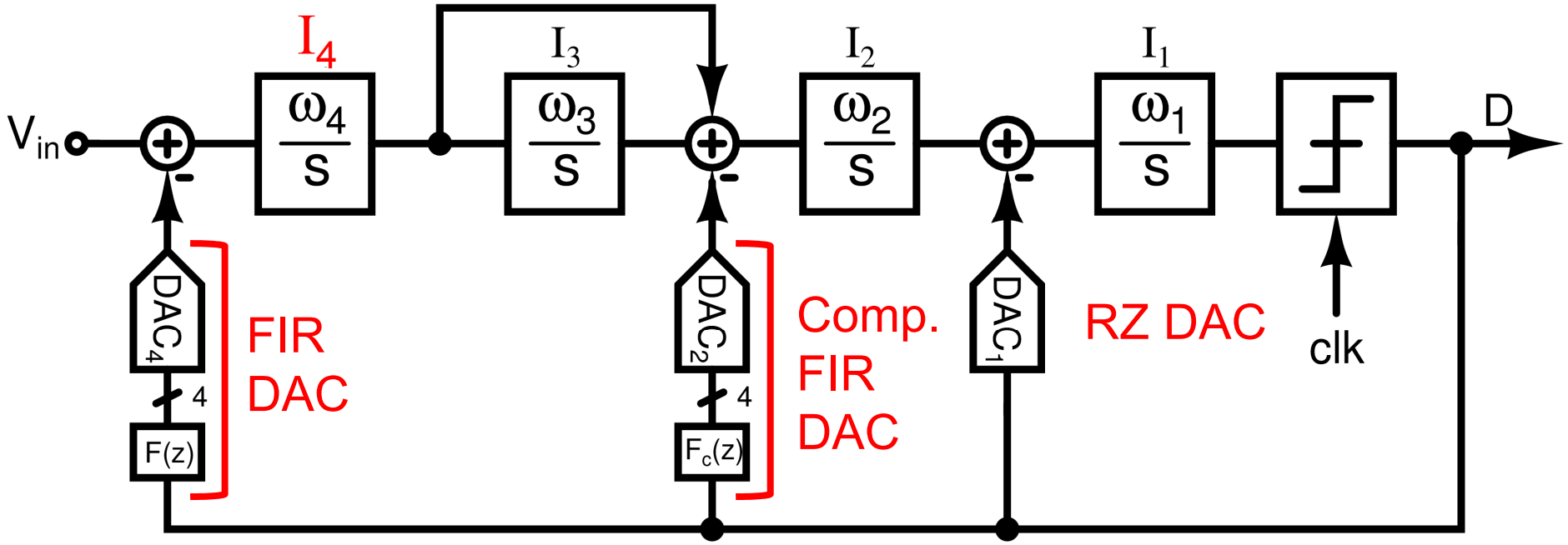
H. Munoz, et. al, "A 4.7mW 89.5dB DR CT Complex ΔΣ ADC with built-in LPF," *Proc. of the ISSCC, Feb. 2005*

CTDSM architecture



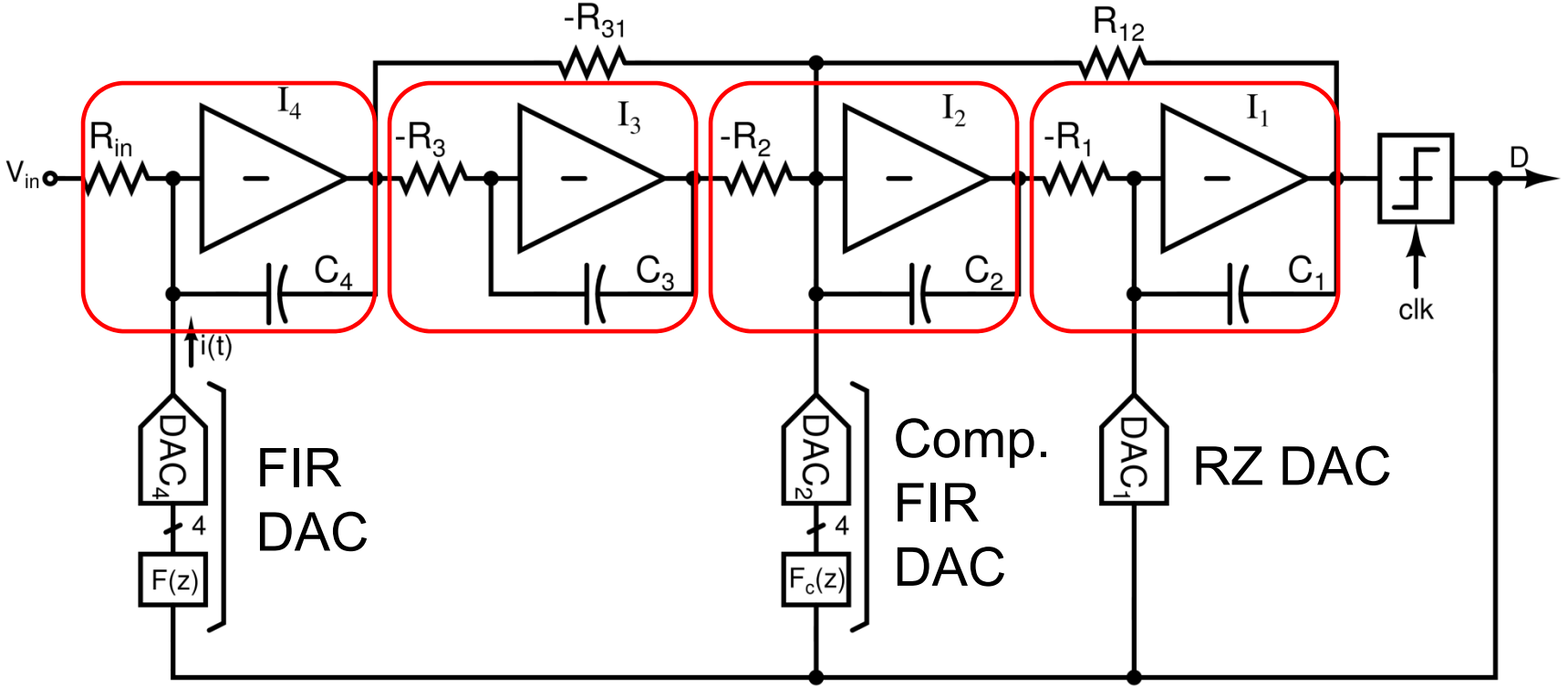
- First order path (through DAC_1 & I_1)
  - DAC_1 is RZ
  - Compensate for excess loop delay

CTDSM architecture



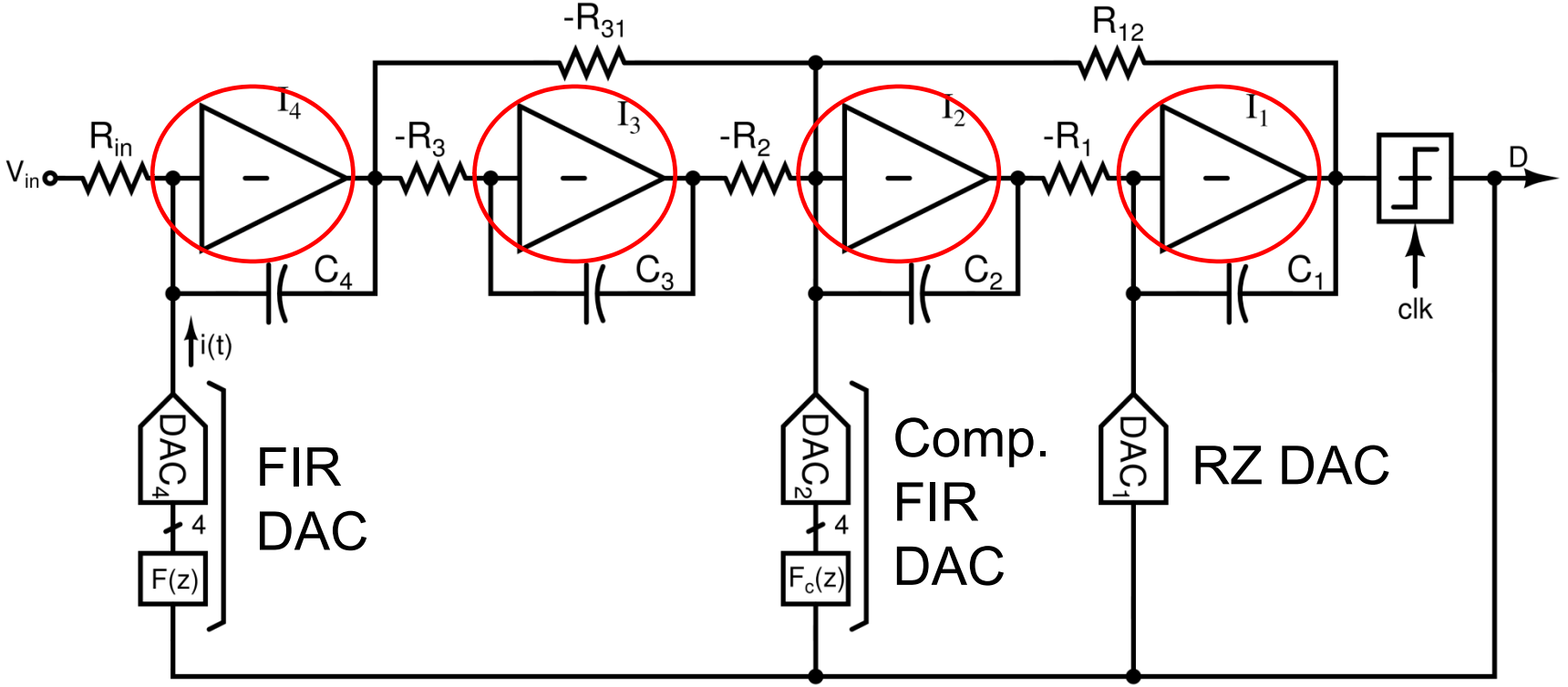
- 4-tap FIR filter used with DAC_4
  - Improves jitter tolerance
  - Reduces linearity requirement on I_4
- $F_c(z)$ compensates for the delay introduced by F(z)

Modulator circuit



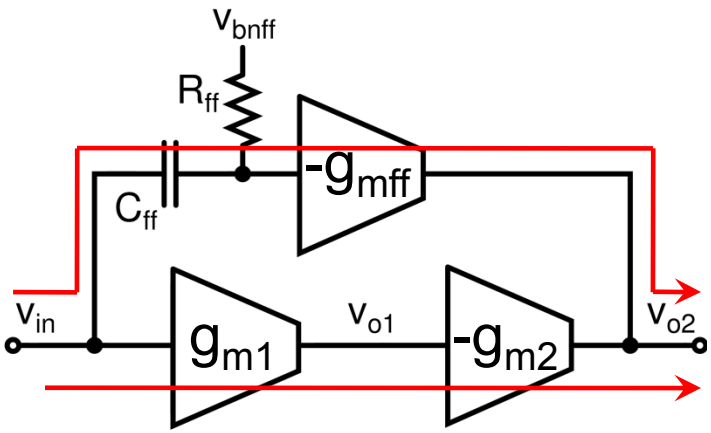
- Active RC integrators

Modulator circuit

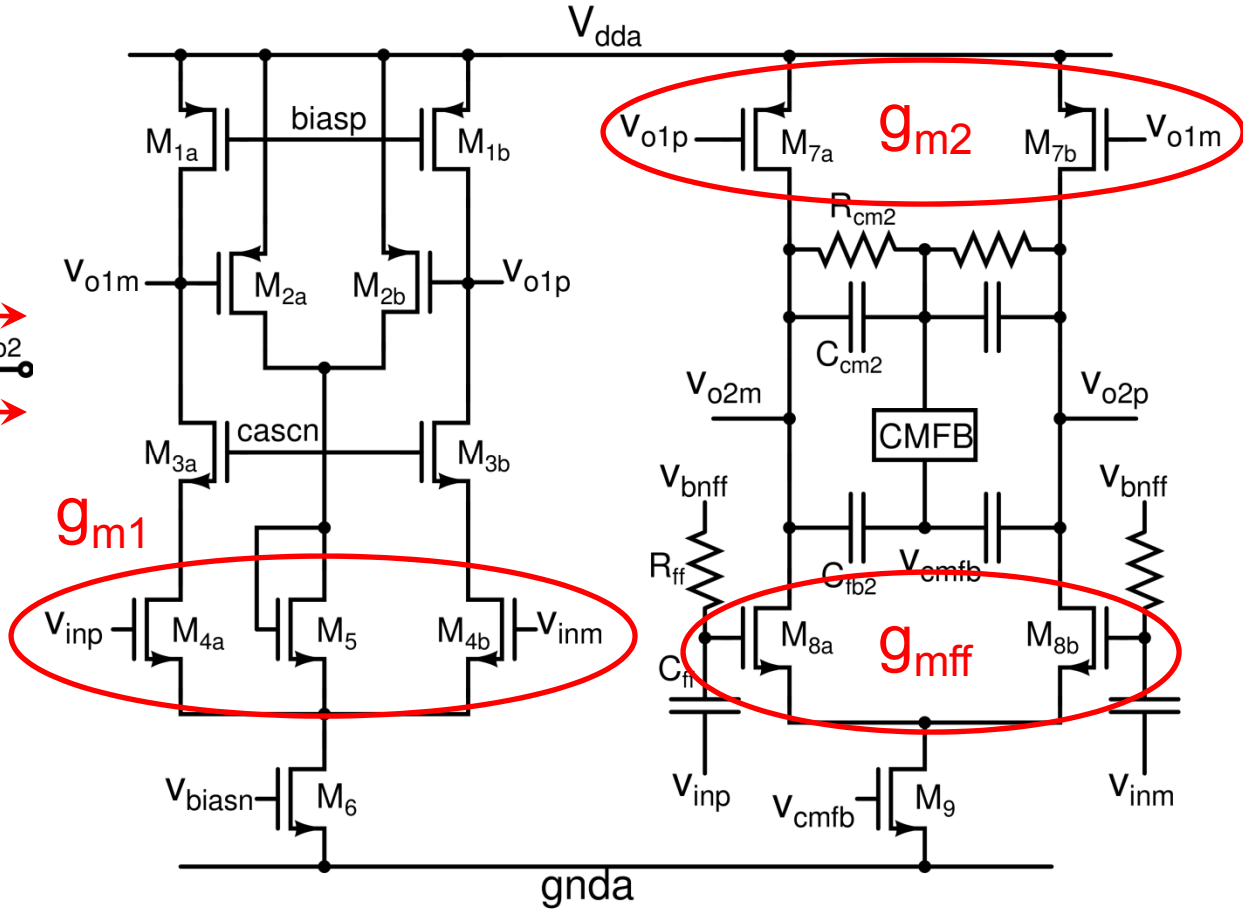


- Active RC integrators
- Feedforward compensated opamp

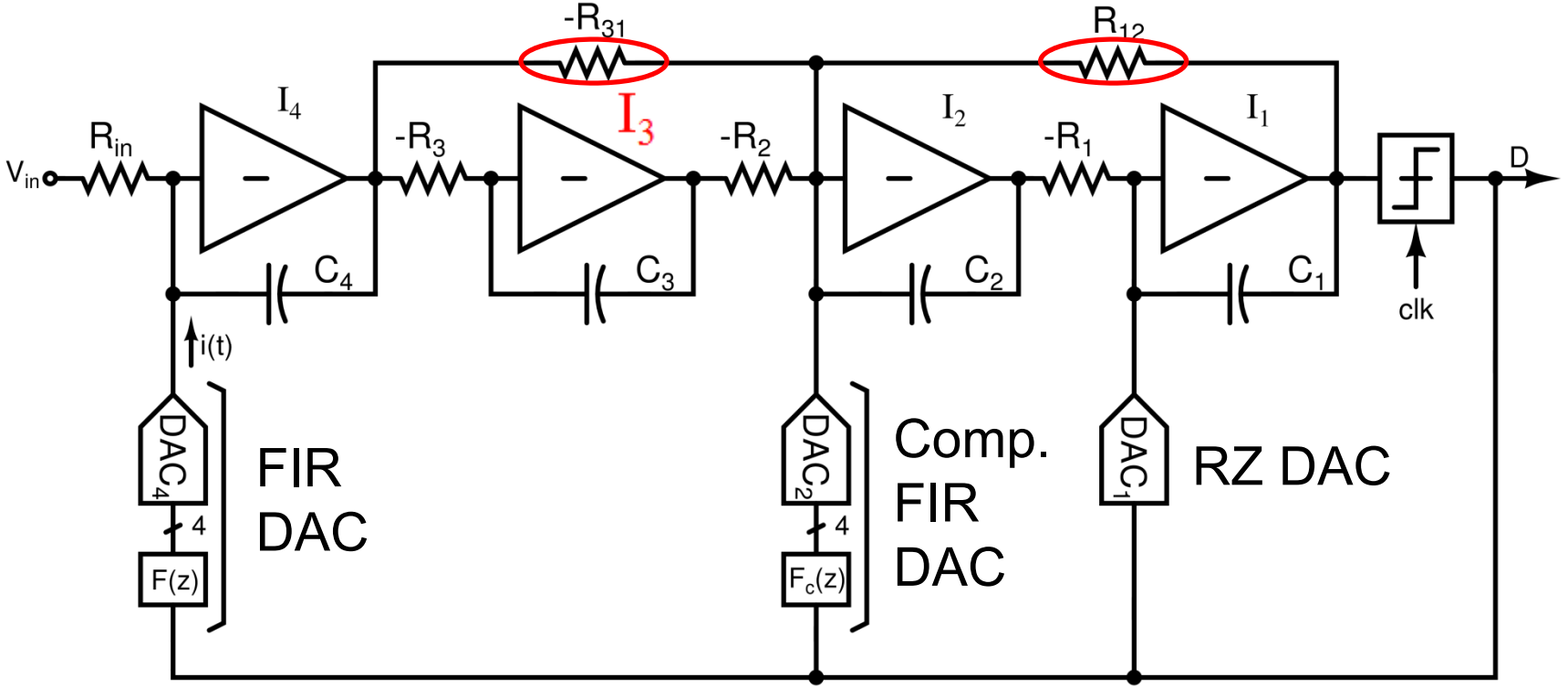
Feedforward compensated opamp



High speed path

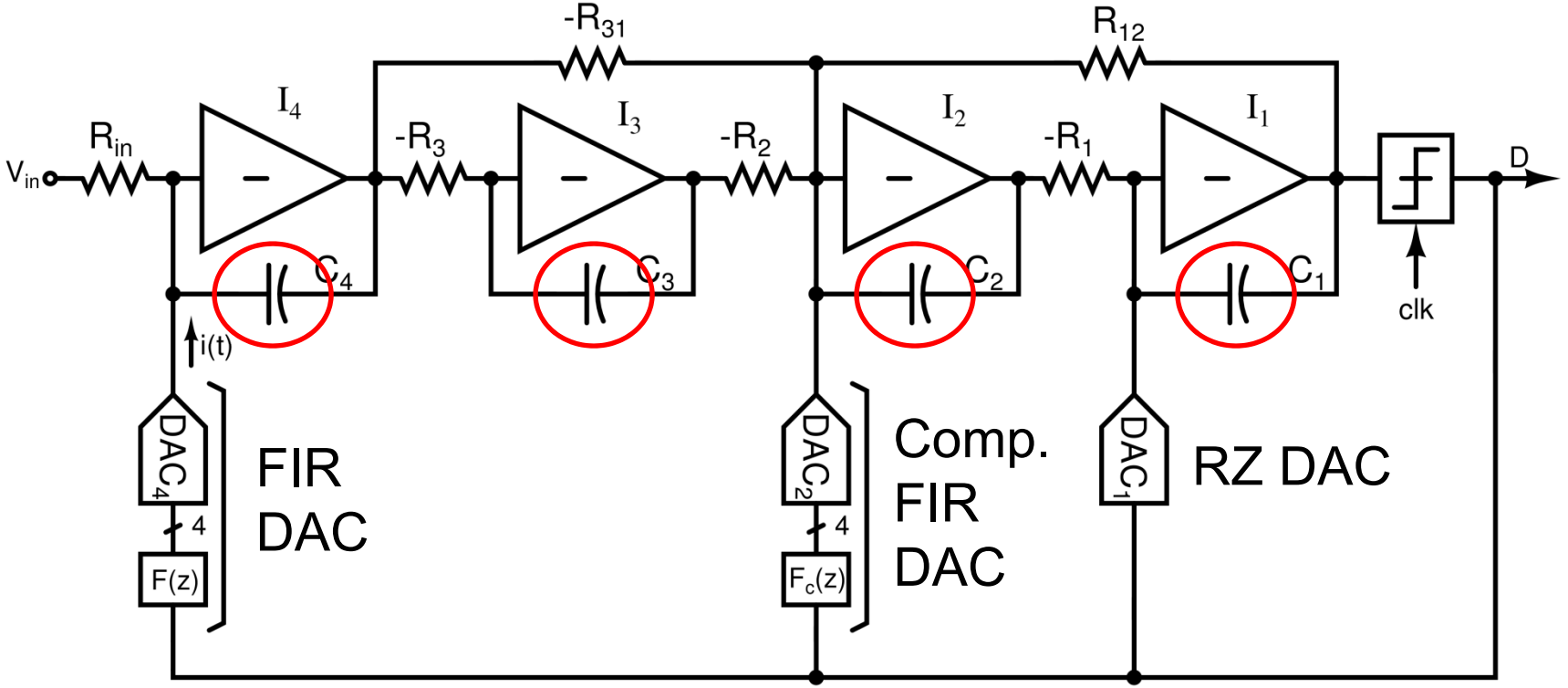


Modulator circuit



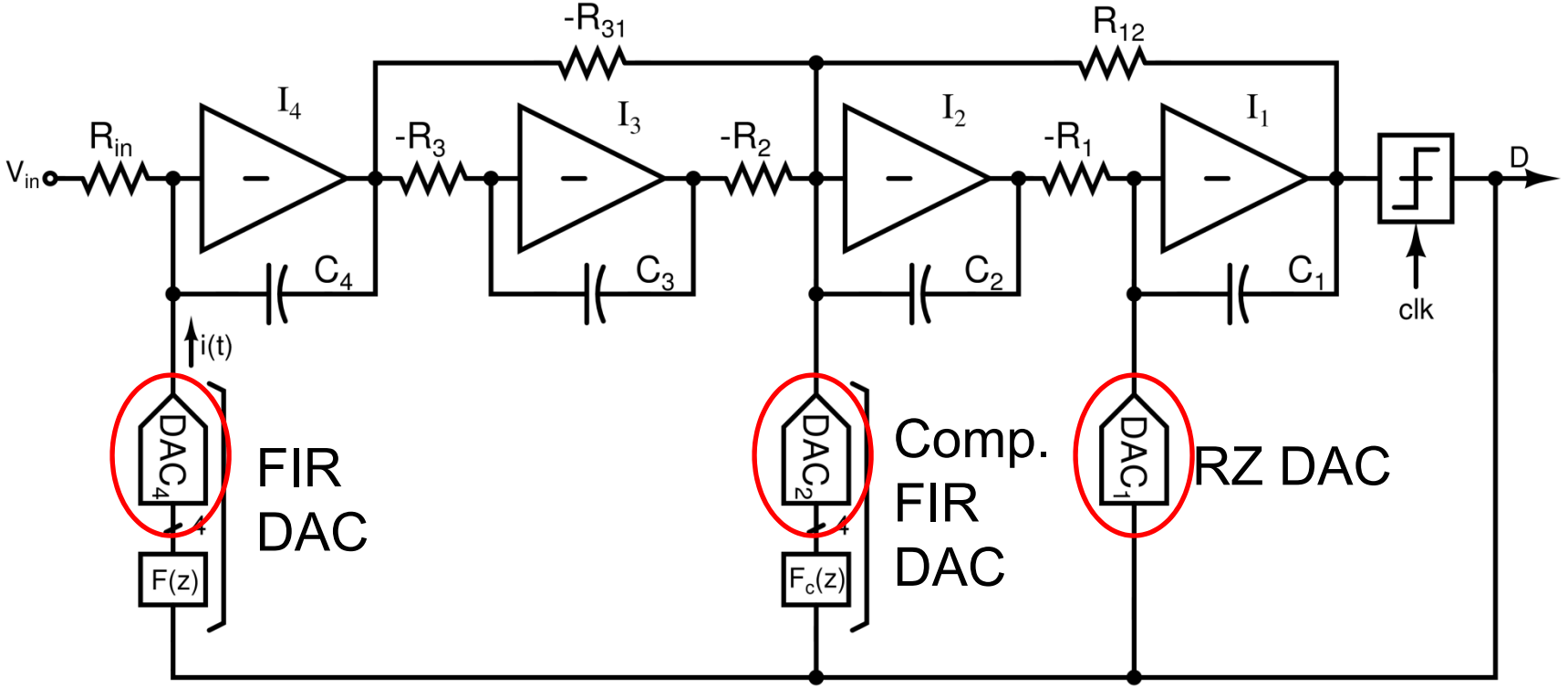
- R_{31} implements feedforward path across I_3
- R_{12} implements the complex zero in the NTF

Modulator circuit



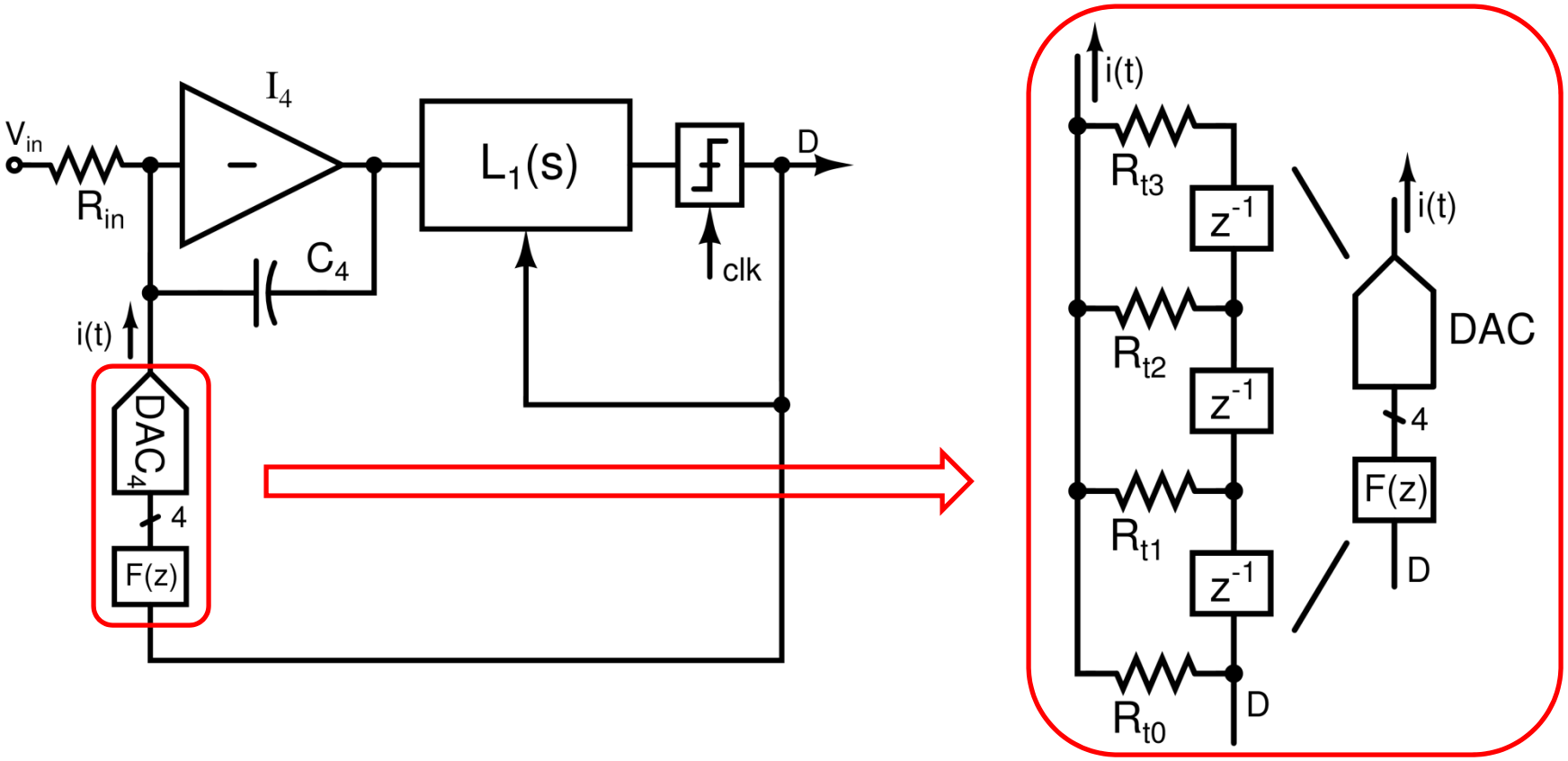
- All capacitors are digitally tunable banks
  - Trim RC time constant variations

Modulator circuit



- All capacitors are digitally tunable banks
  - Trim RC time constant variations
- All DACs are resistive → low noise

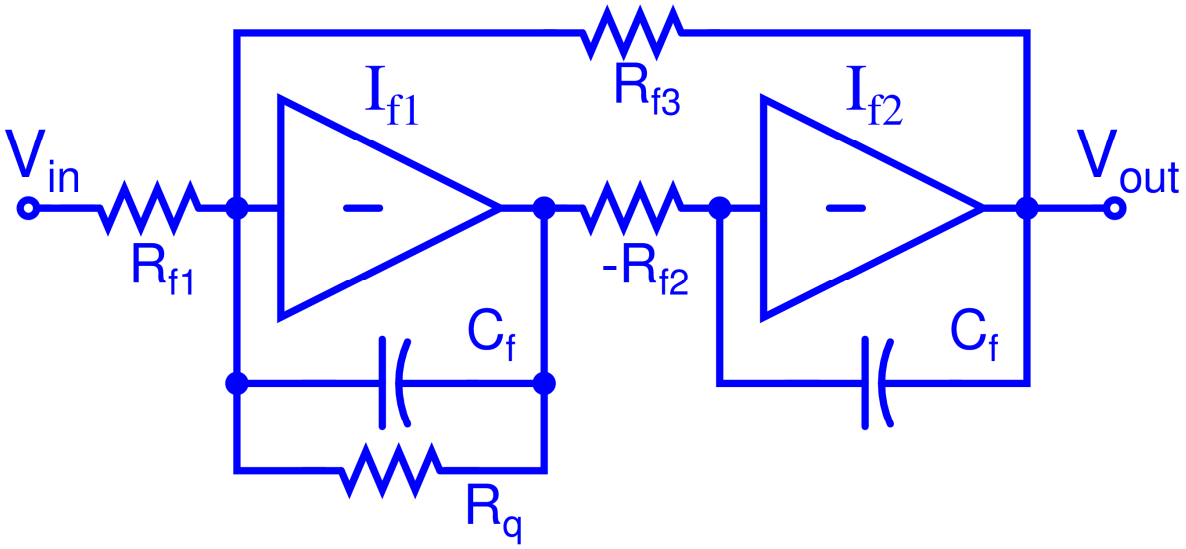
FIR DAC



- FIR DAC implemented using semi-digital techniques

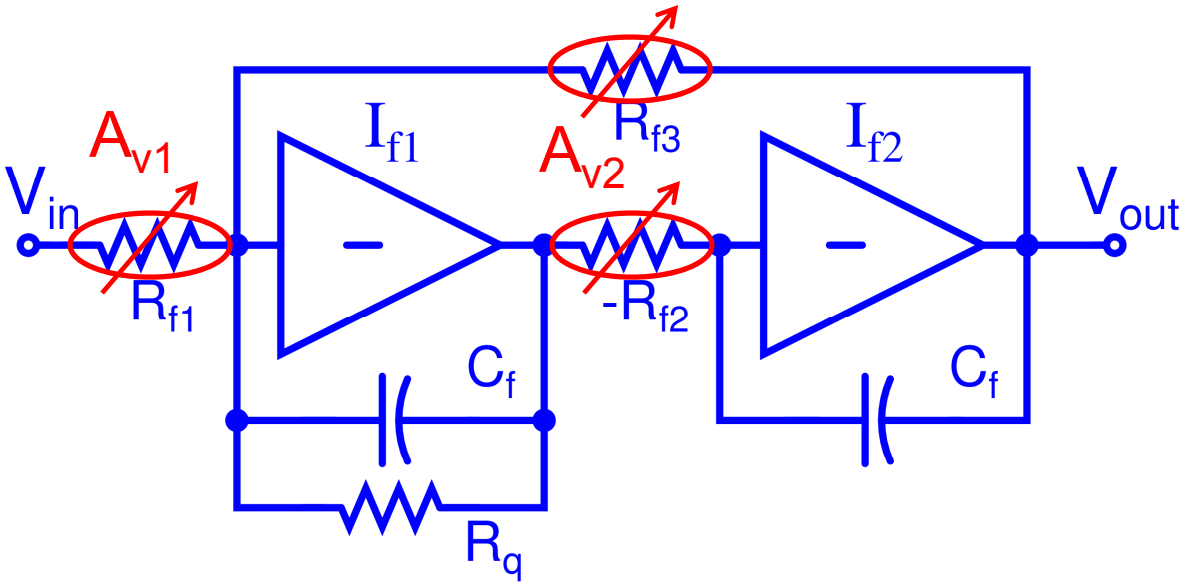
- D. K. Su, et. al, "A CMOS oversampling D/A converter with a current mode semi-digital reconstruction filter," in *IEEE JSSC*, Dec. 1993.

Filter



- Second order Butterworth filter
- Active RC implementation
- 3 dB bandwidth = 4 MHz

Filter upfront (H_1-ΔΣ)

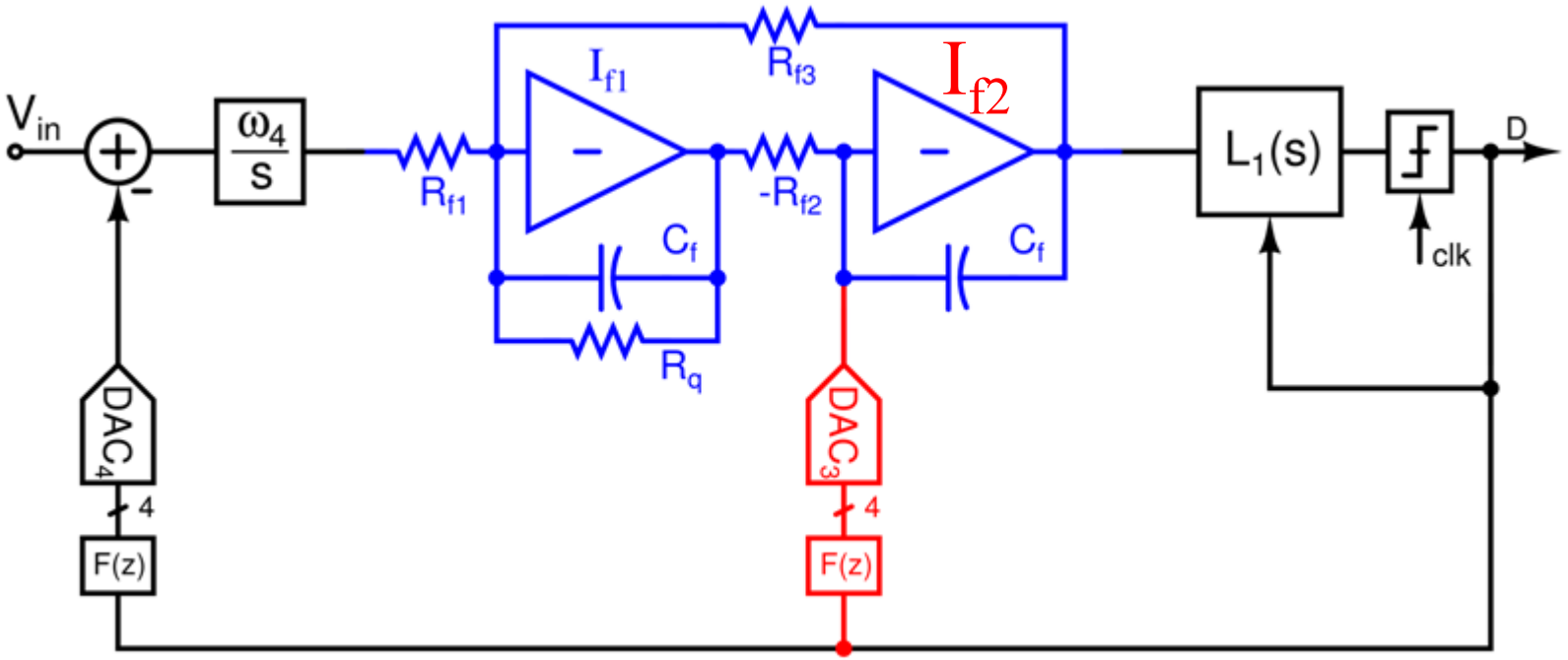


- VGA implemented in two stages
- A_{v1} (0 to 12 dB)
- A_{v2} (0 to 6 dB)

CTDSM with embedded filter

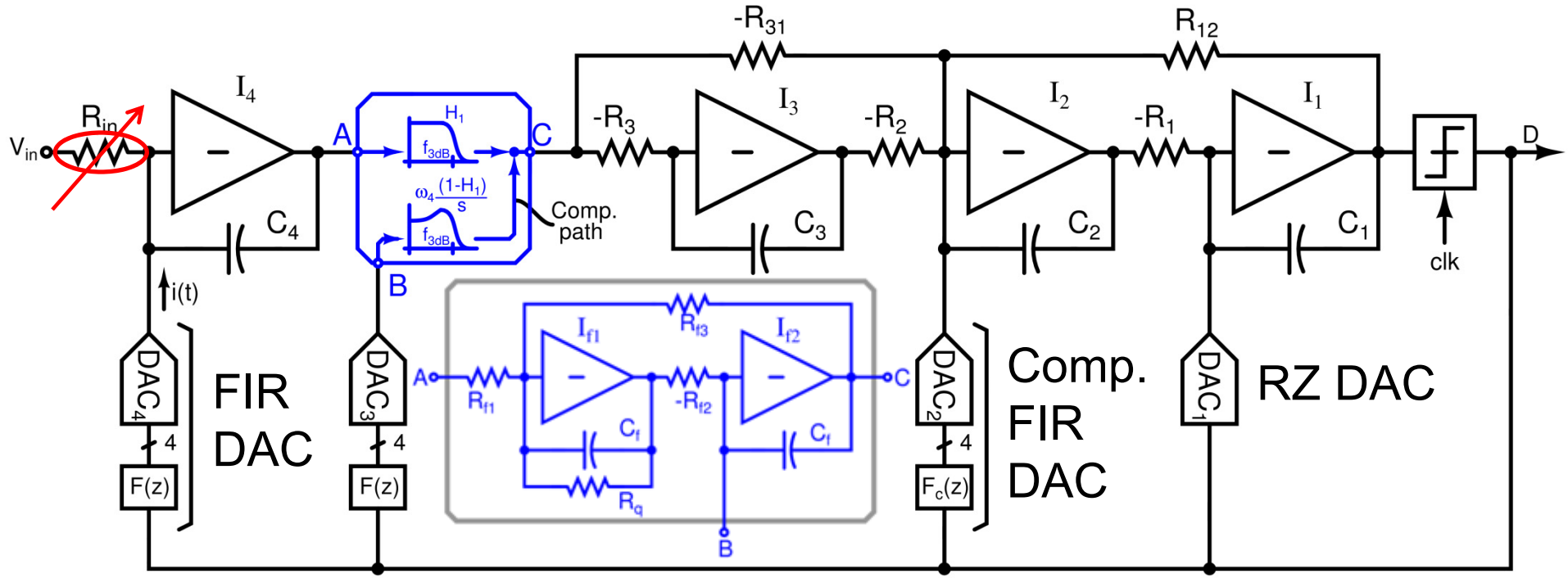
Δ-H_1-Σ

Filter and compensation filter



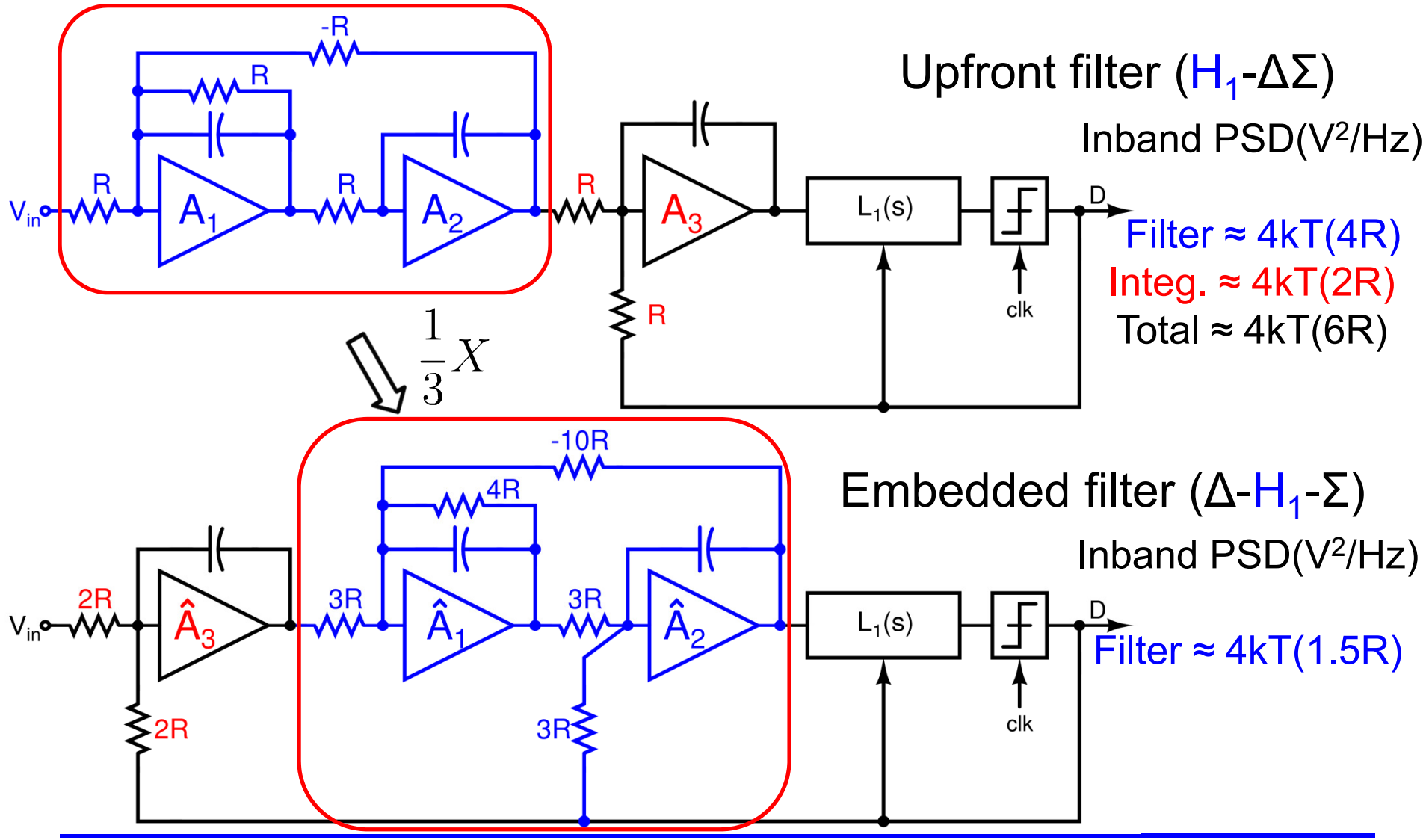
- Second order filter (H_1)
- DAC_3 feeding into I_{f2}
  - Implements compensation filter

Embedded filter circuit (Δ-H_1-Σ)

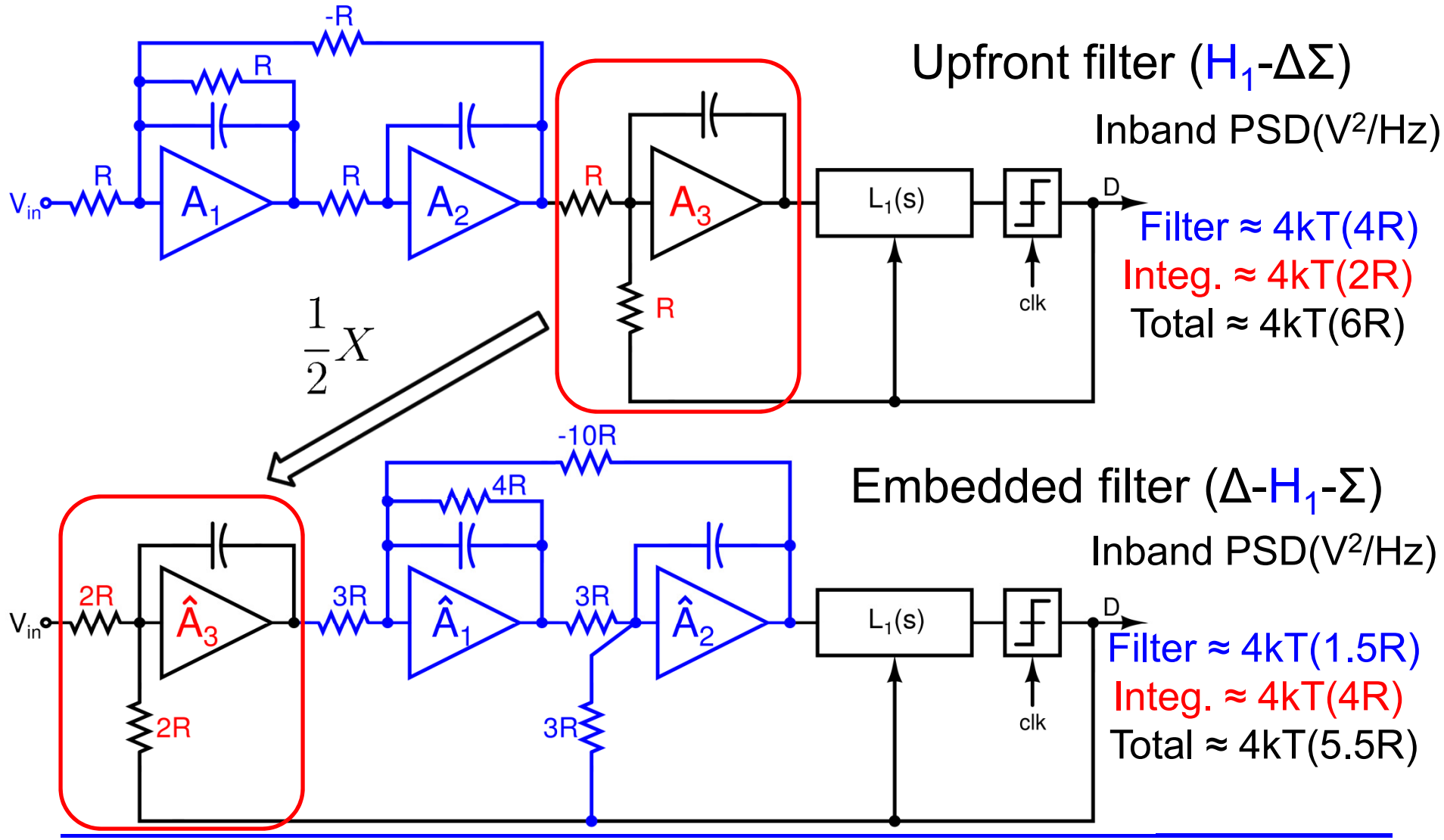


- Varying R_{in} implements the VGA (0 to 18 dB)

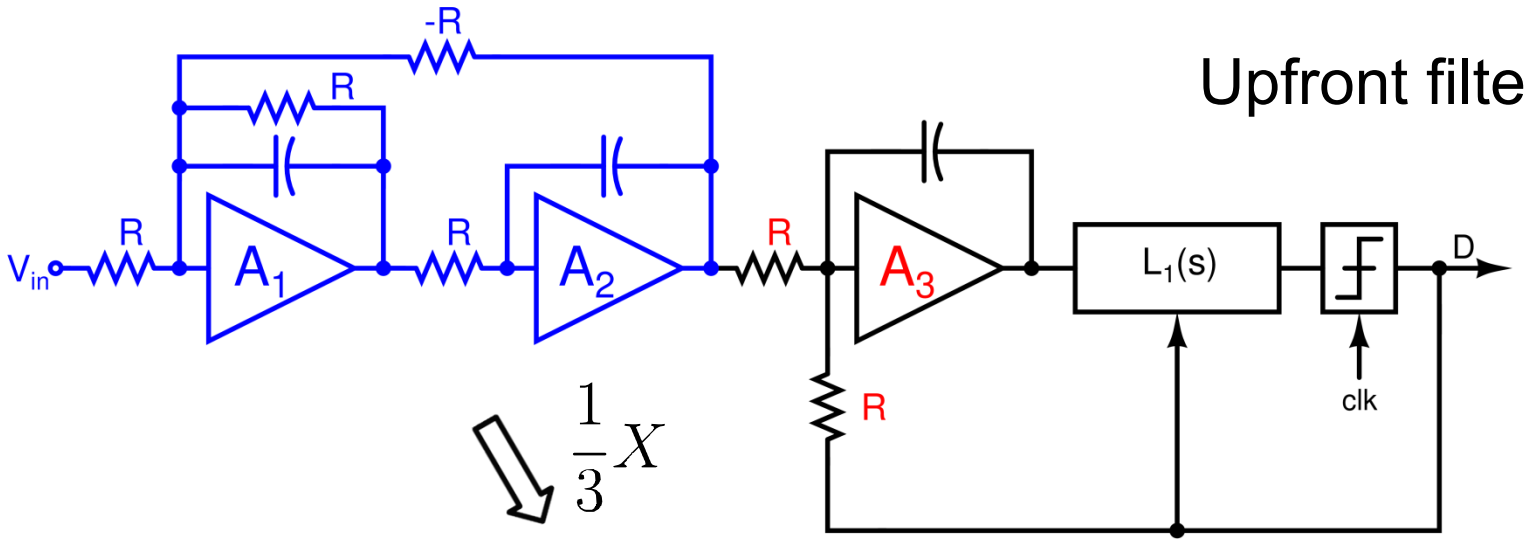
Impedance levels

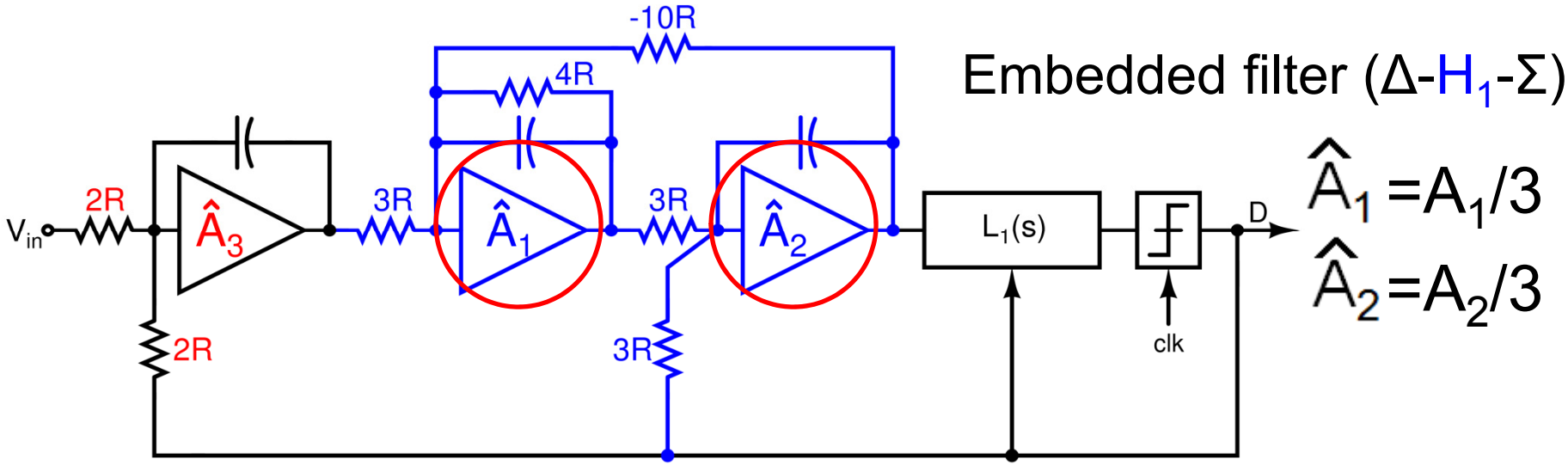


Impedance levels

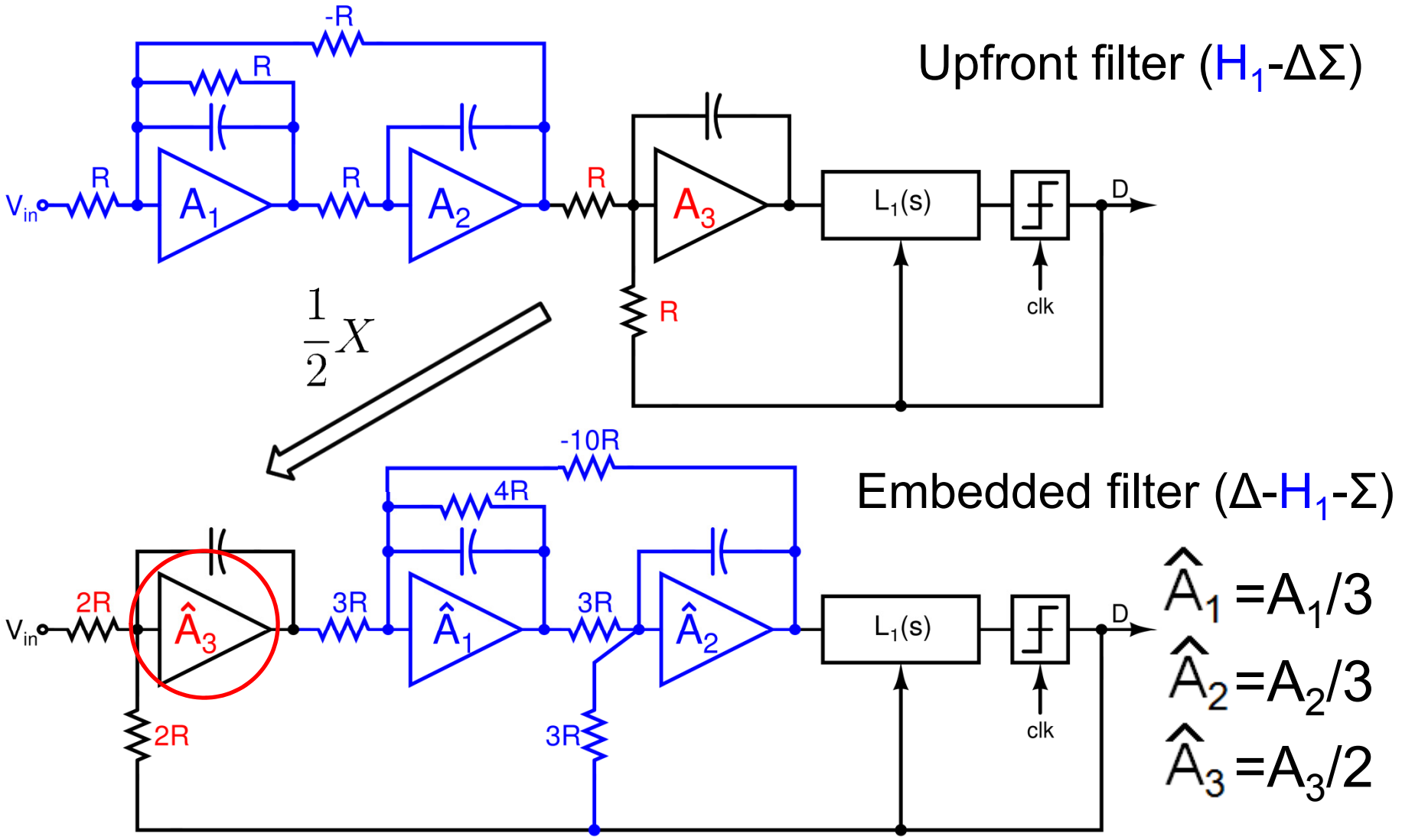


Opamp currents (Δ-H_1-Σ)



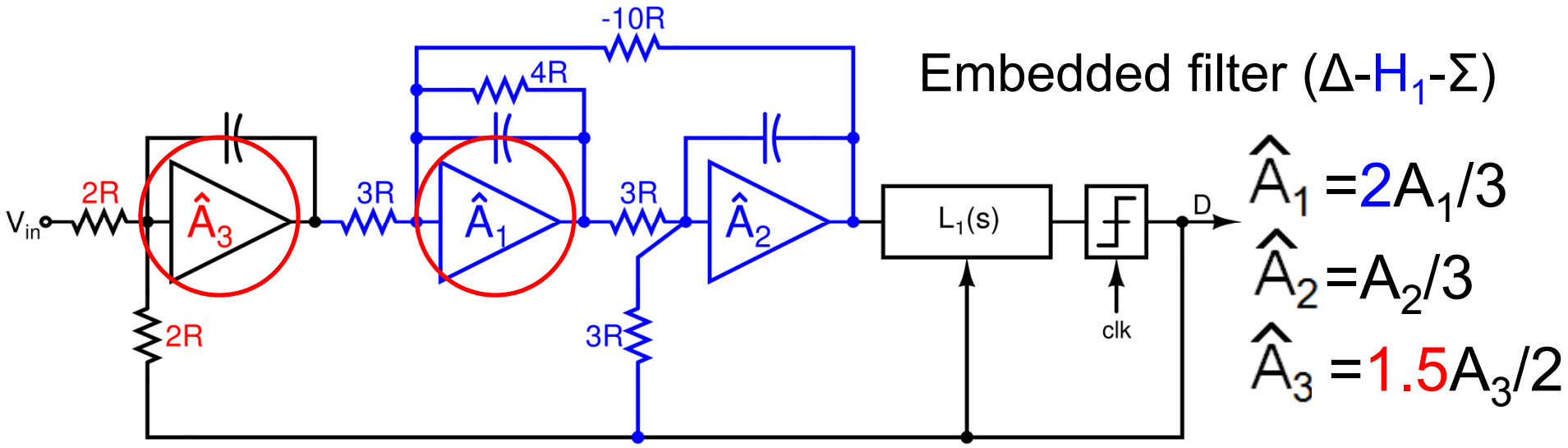


Opamp currents (Δ-H_1-Σ)

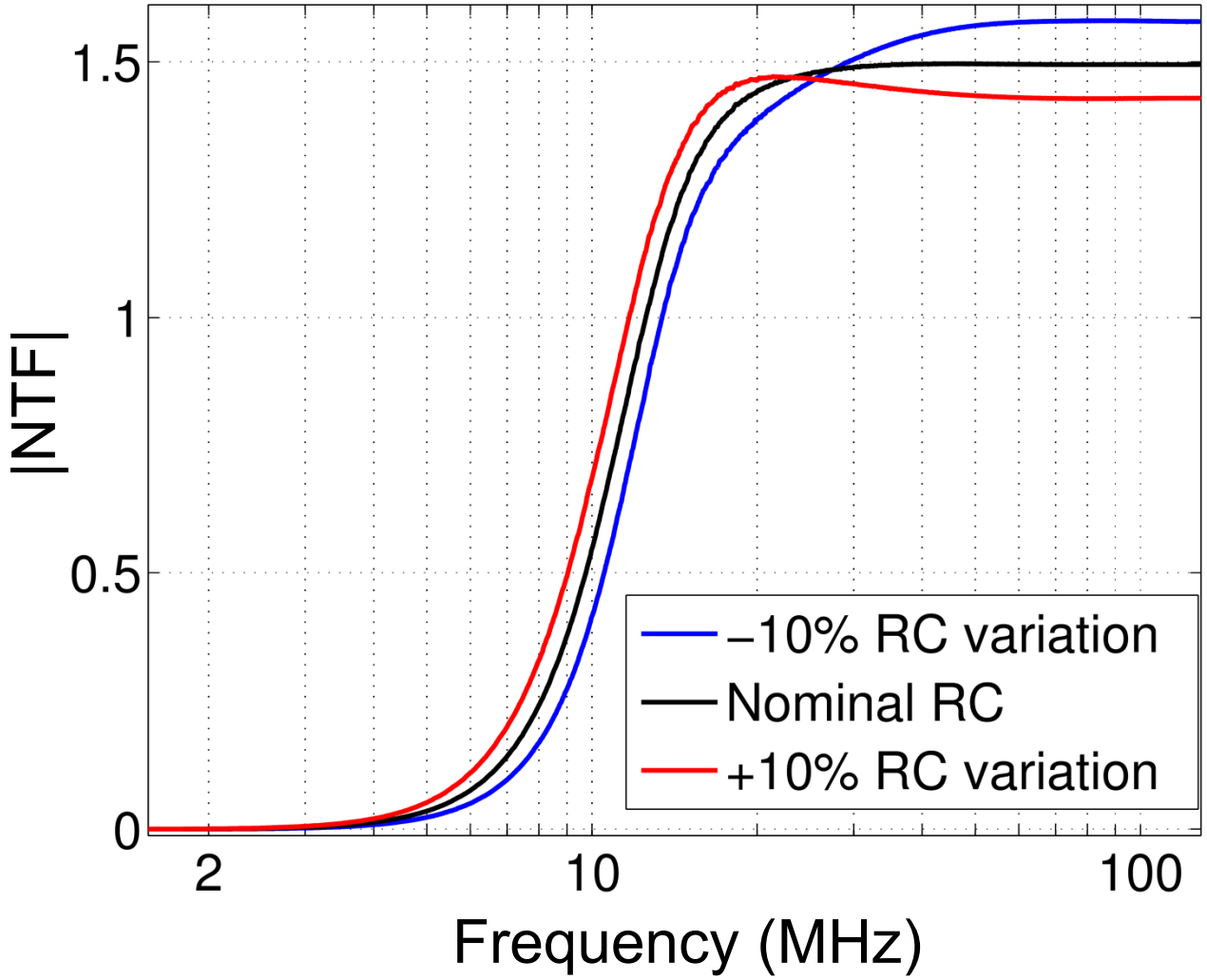


Opamp currents (Δ-H_1-Σ)

- Distortion depends on G_mR
- Currents in $\hat{A}_1$, $\hat{A}_3$ increased to improve linearity



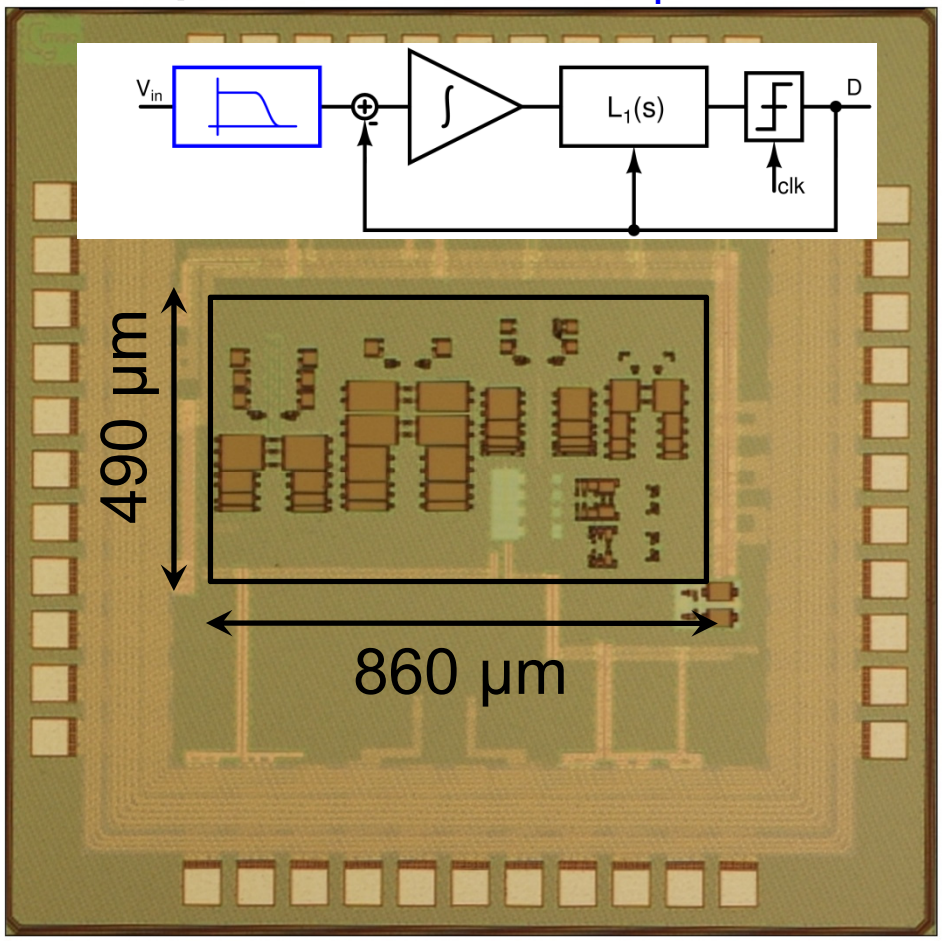
RC time constant variation



Measurement Results

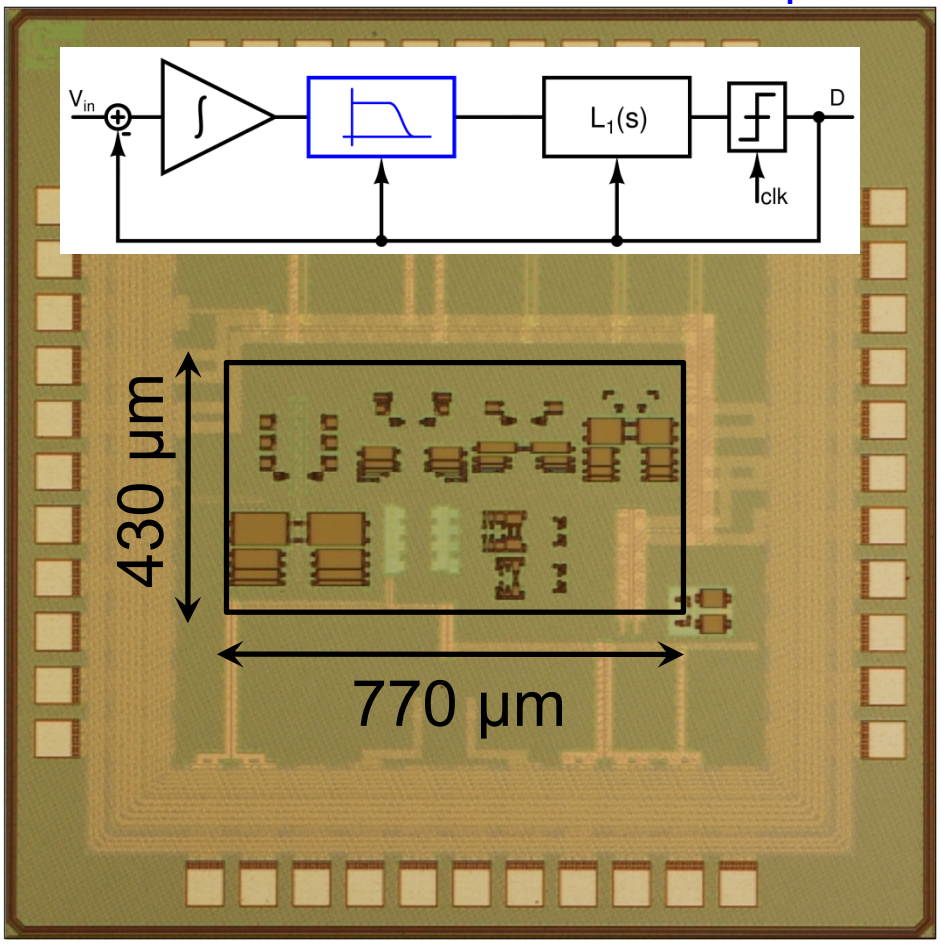
Die photograph

Upfront filter : H_1- ΔΣ



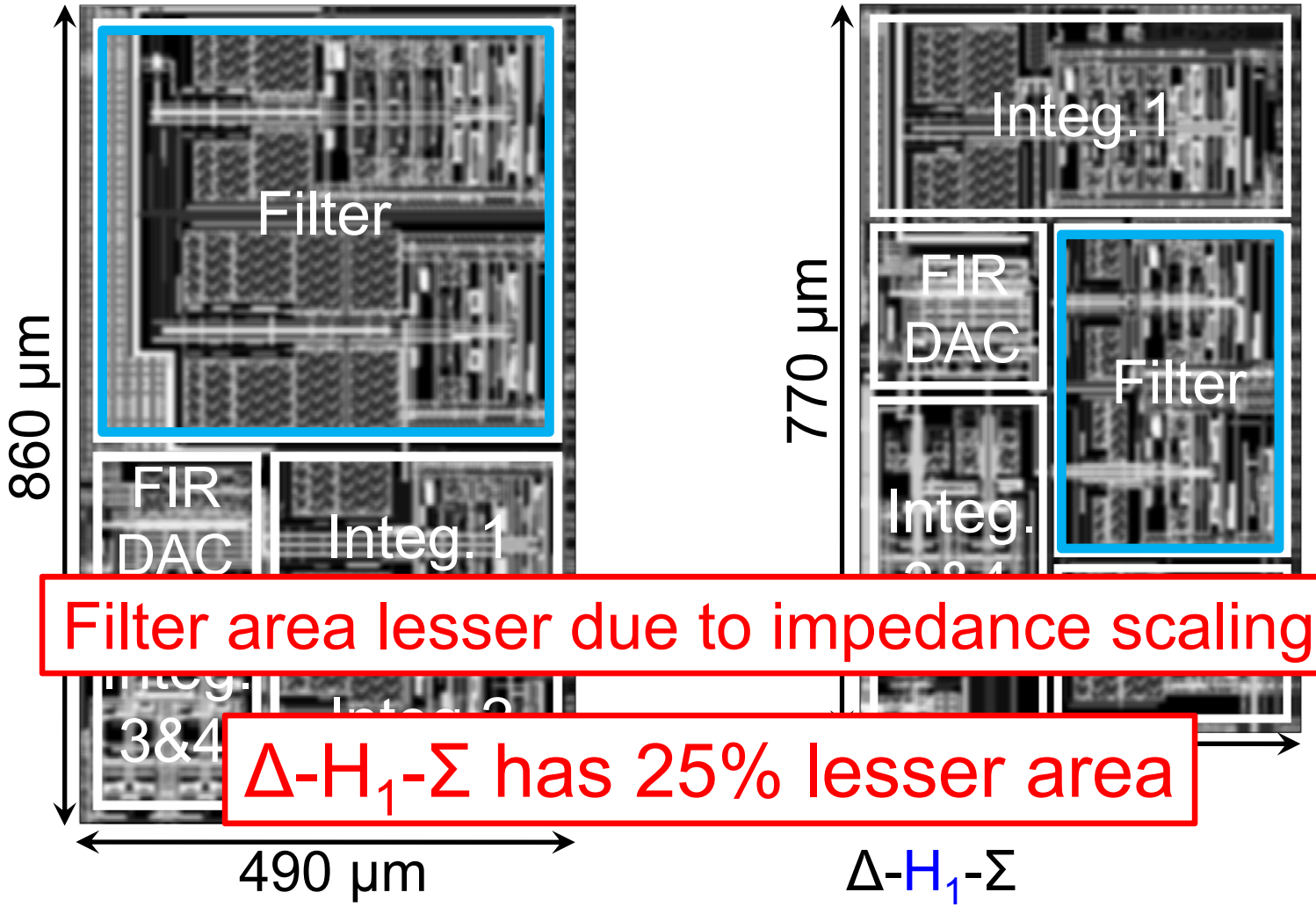
Active area = 0.42mm²

Embedded filter : Δ-H_1-Σ



Active area = 0.33mm²

Layout of the modulators



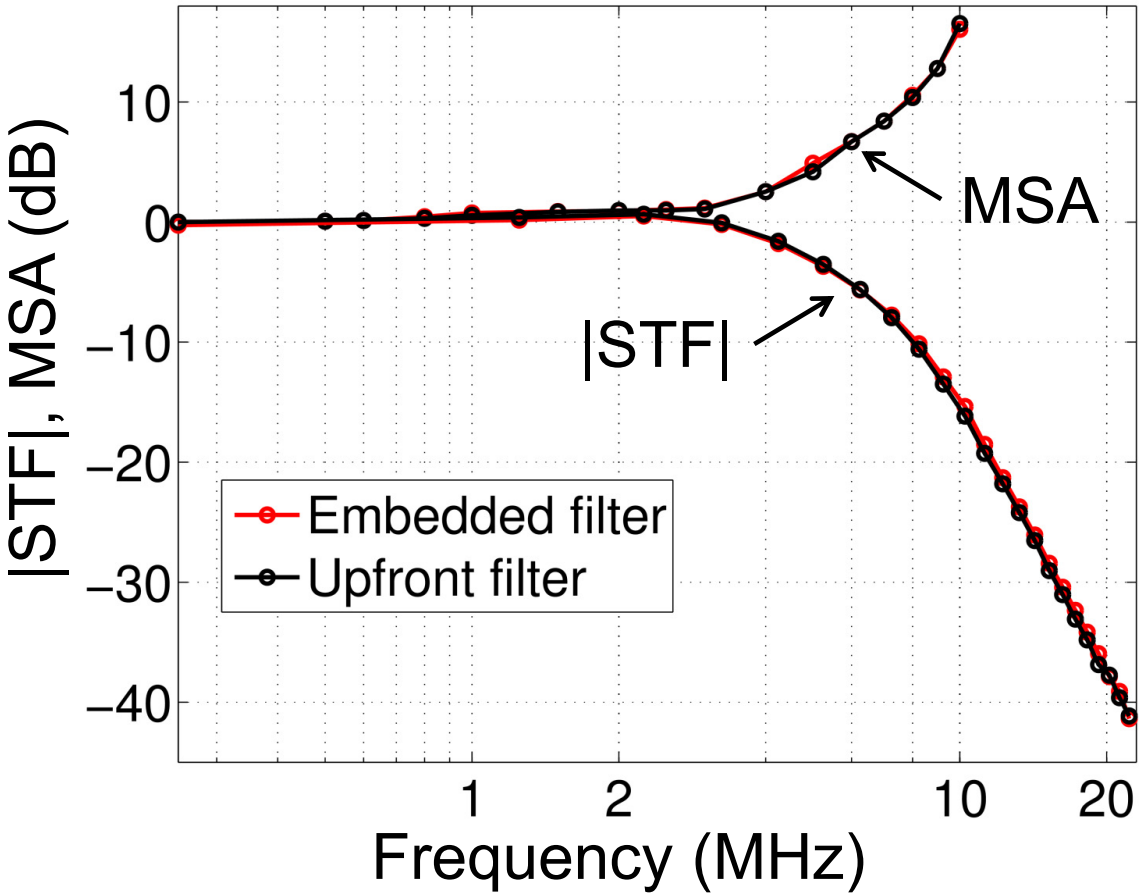
Filter area lesser due to impedance scaling

Δ-H_1-Σ has 25% lesser area

H_1- ΔΣ Active area = 0.42mm²

Δ-H_1-Σ
Active area = 0.33mm²

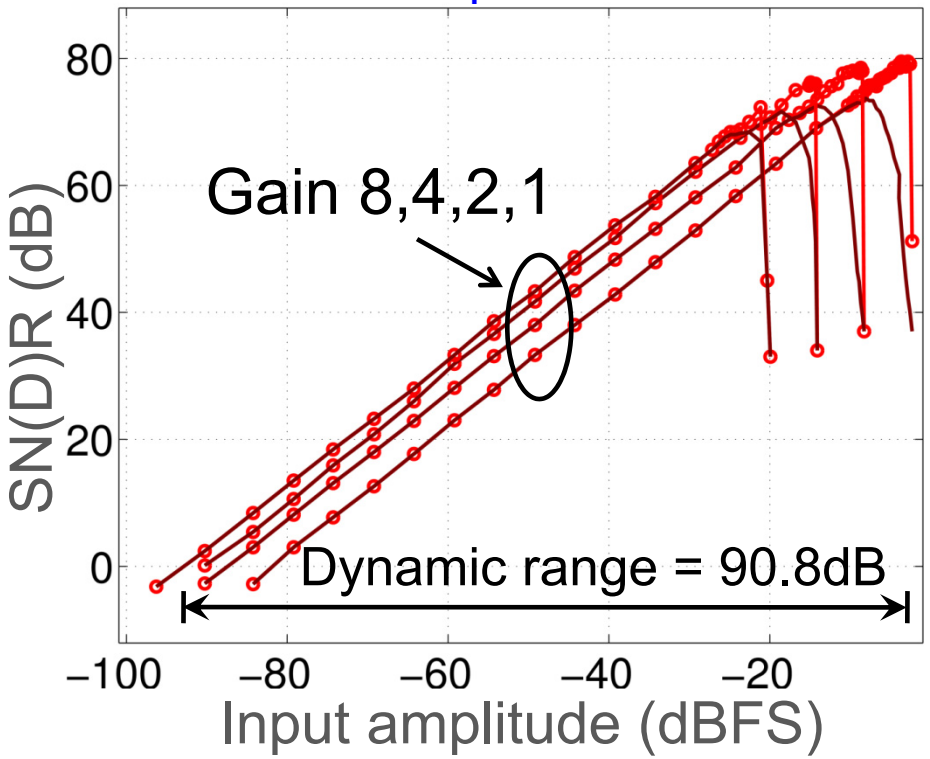
STF and MSA



- STF : Signal transfer function
- MSA : Maximum stable amplitude

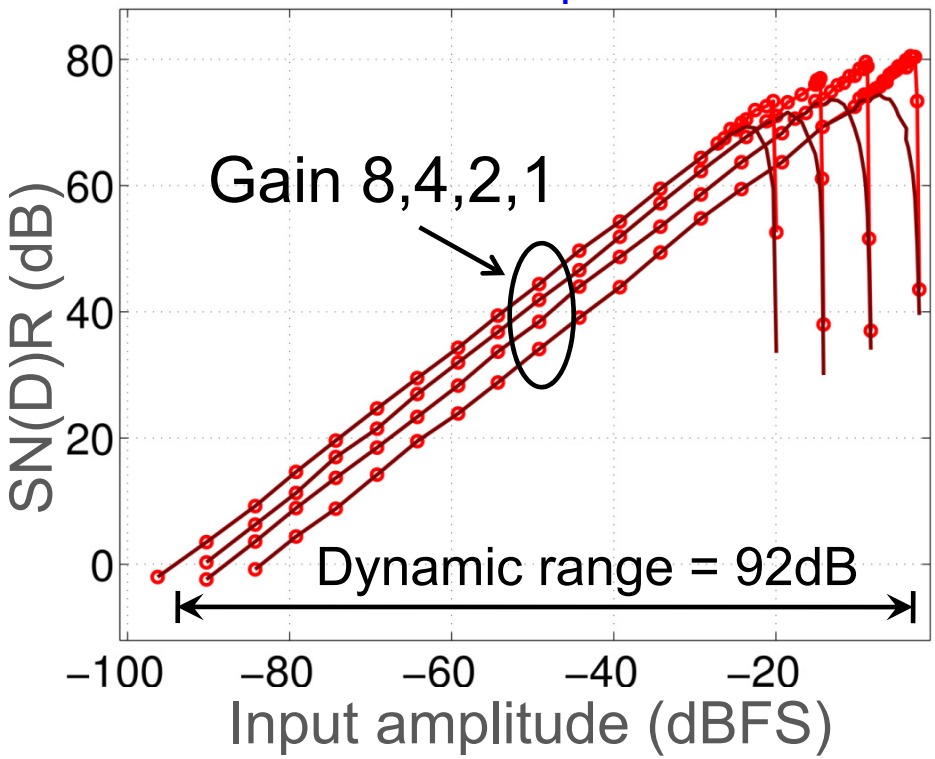
SNR vs Amplitude

H_1- ΔΣ



- SNR_{max} / DR = 79.5 / 81 dB
- Power = 6.8 mW

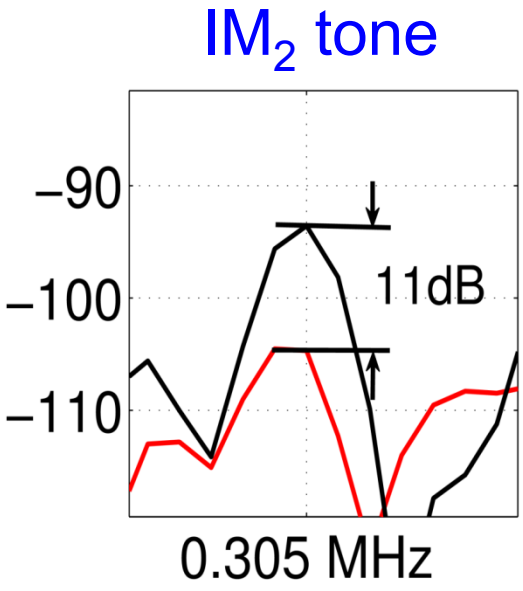
Δ-H_1-Σ

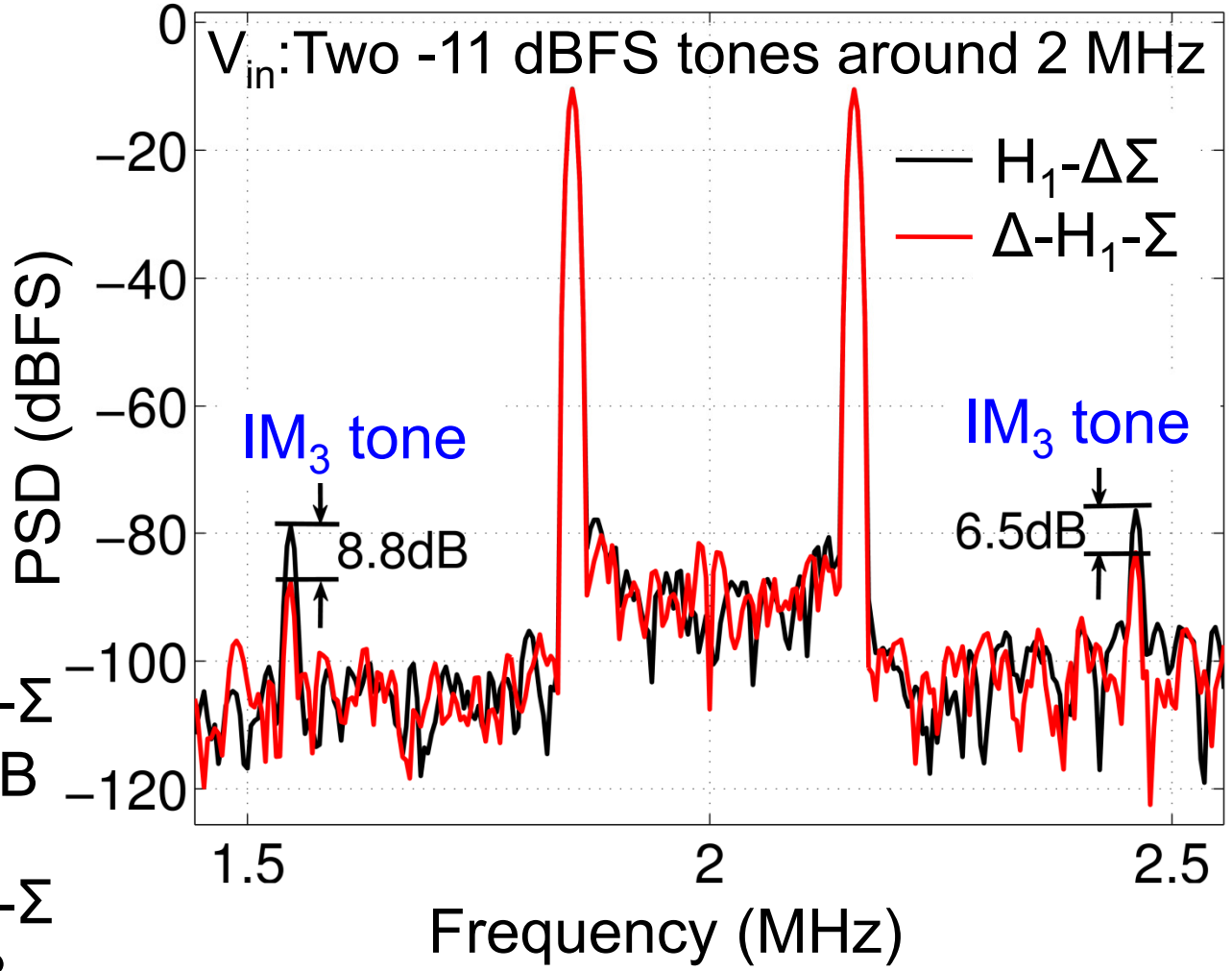


- SNR_{max} / DR = 80.5 / 82 dB
- Power = 5 mW

Linearity Measurements

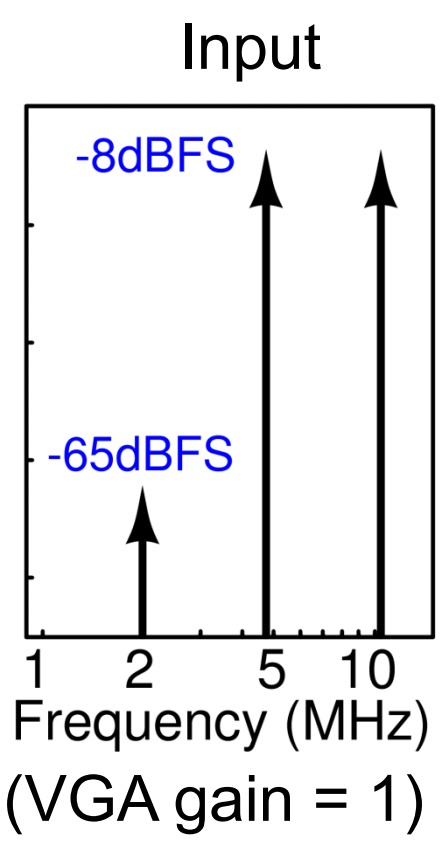
Inband IM_3/IM_2

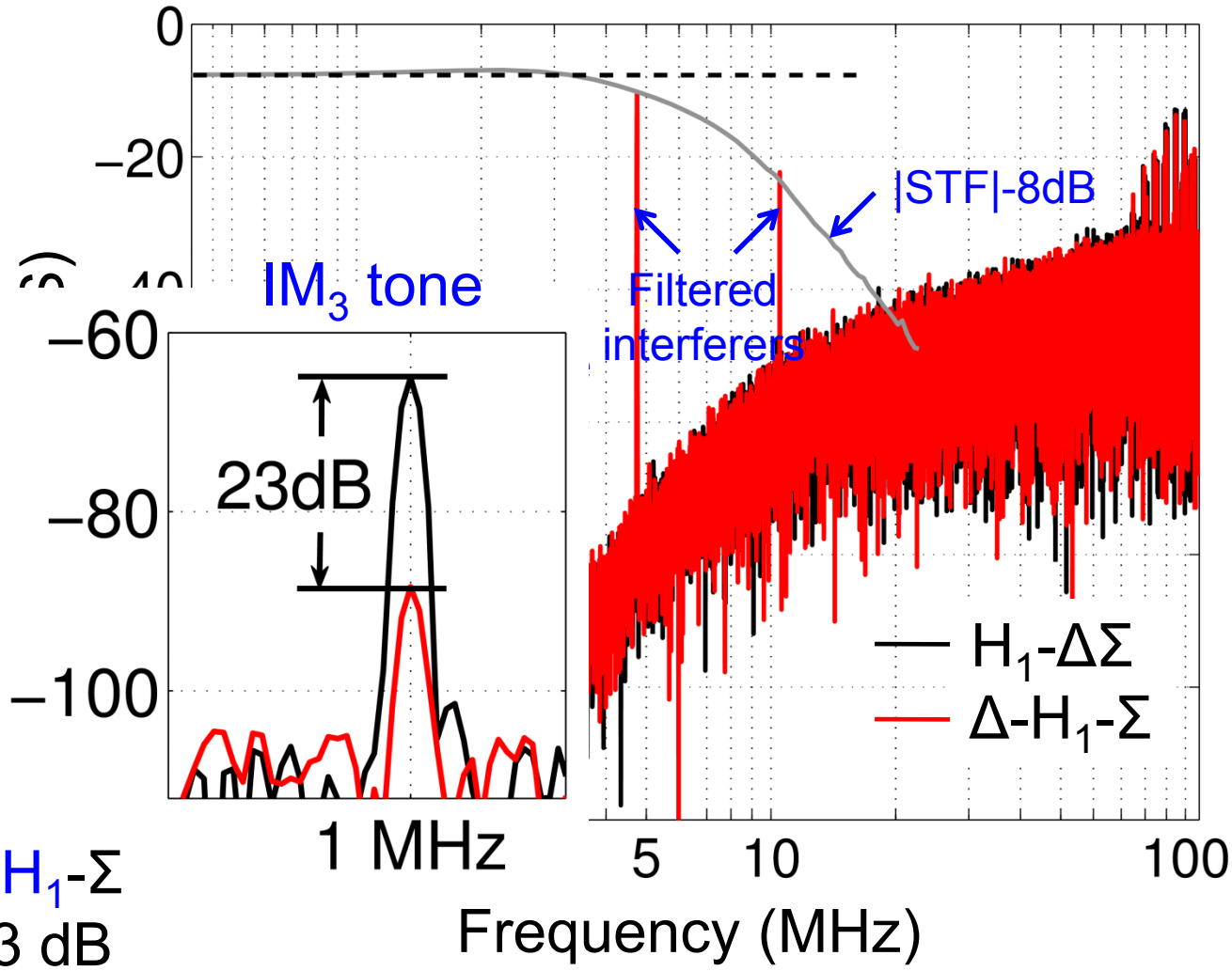




- IM_2 tone of Δ-H_1-Σ lesser by ≈ 11 dB
- IM_3 tone of Δ-H_1-Σ lesser by ≈ 7 dB

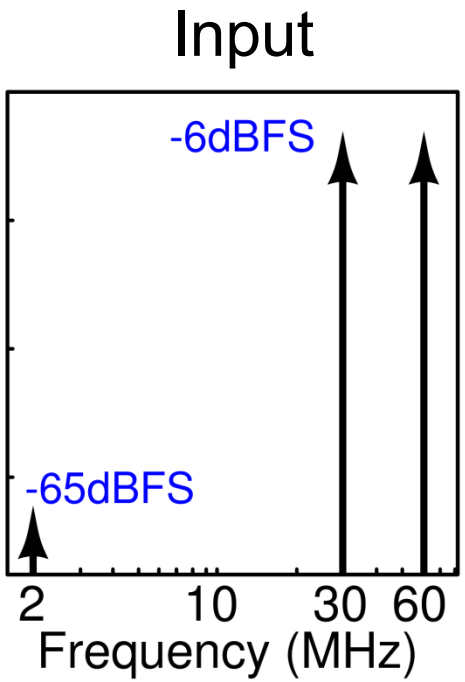
Out-of-band IM_3



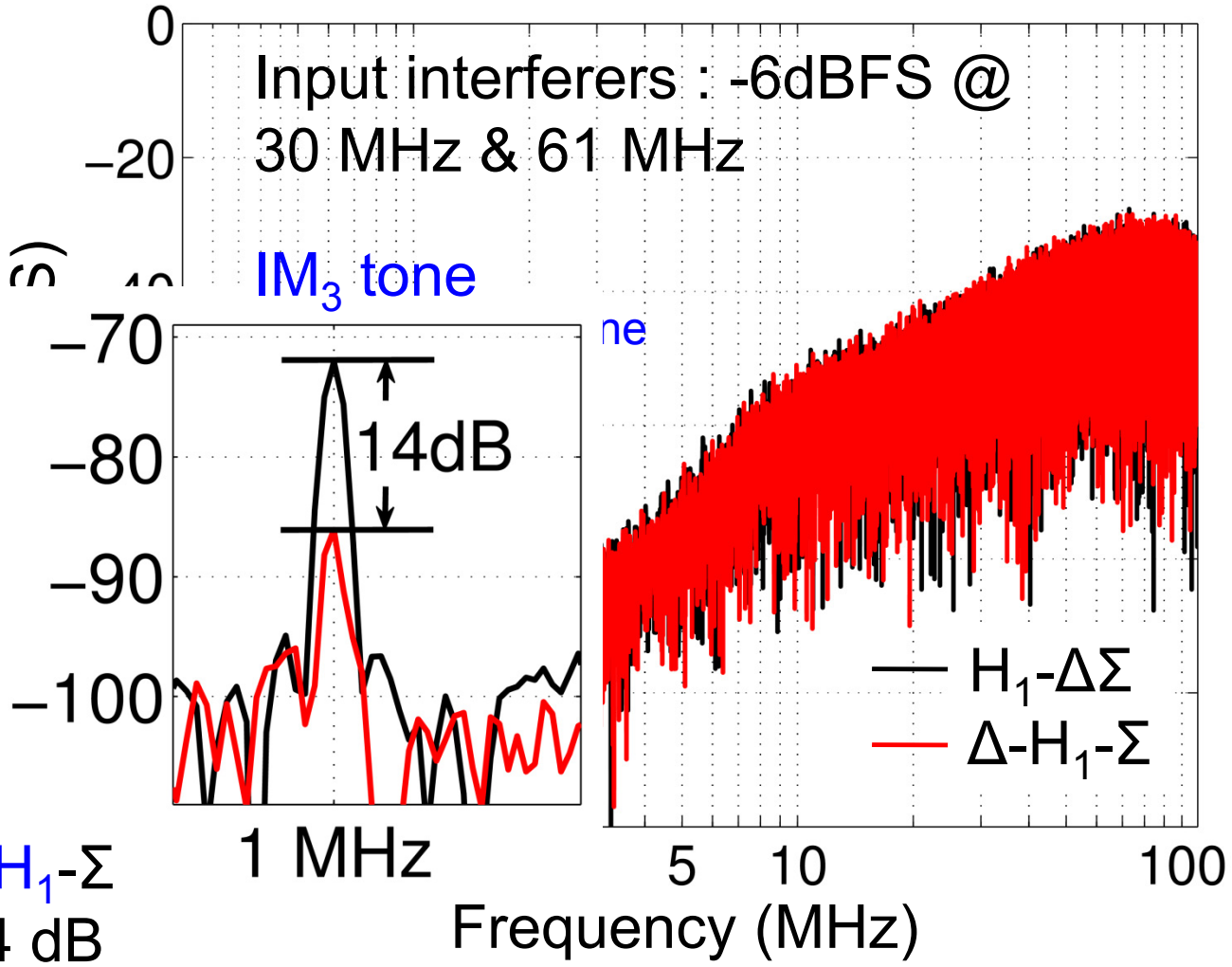


- IM_3 tone of Δ-H_1-Σ lesser by ≈ 23 dB

Out-of-band IM_3



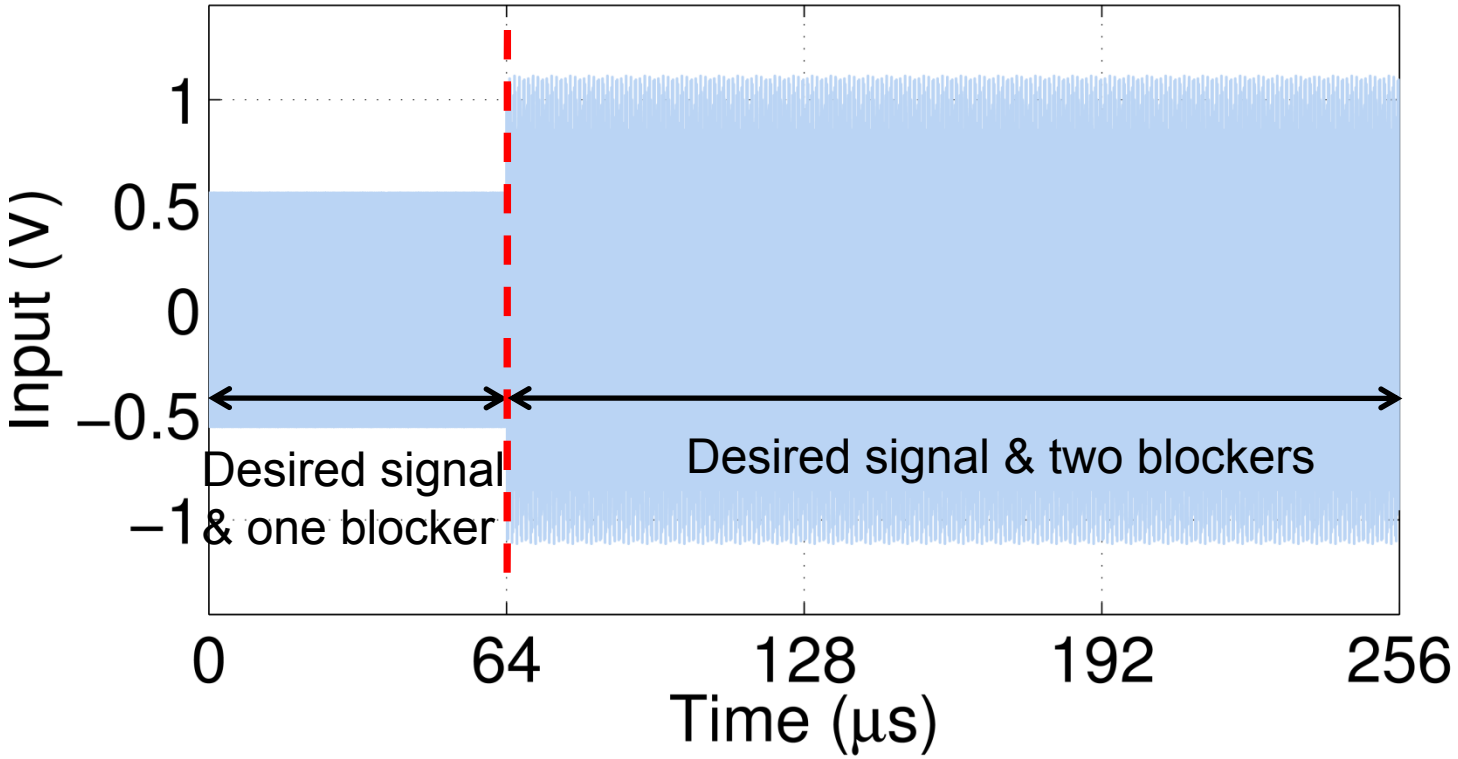
(VGA gain = 4)



- IM_3 tone of Δ-H_1-Σ lesser by ≈ 14 dB

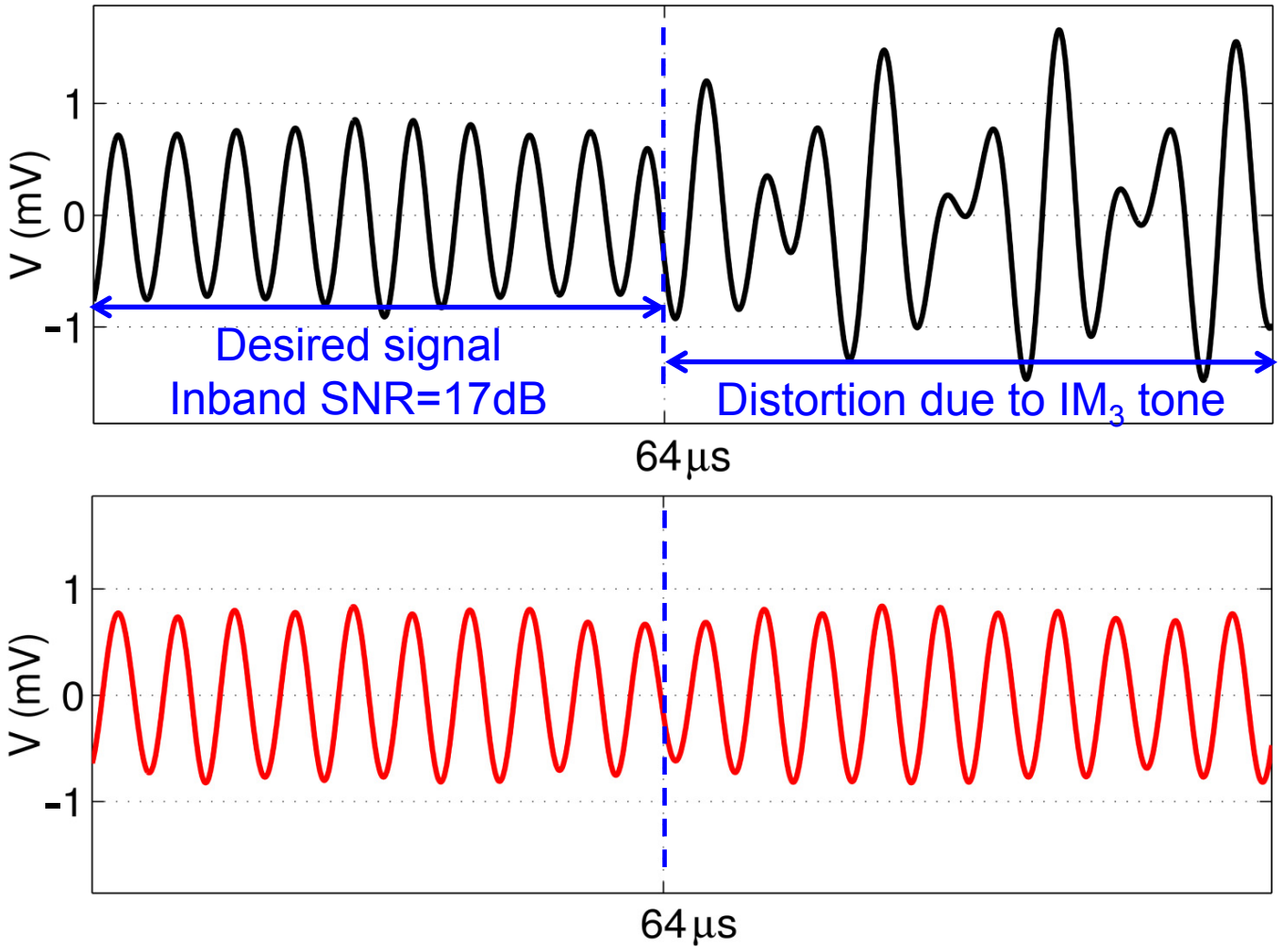
Time domain measurement

Input to the modulators



- IM_3 tone from the blockers fall inband
- Modulator output decimated in software

Decimated modulator output



Upfront filter

H_1-ΔΣ

Δ-H_1-Σ

Embedded filter

Performance summary

	Upfront filter H_1-ΔΣ	Embedded filter Δ-H_1-Σ
Signal BW / f_s	2 MHz / 256 MHz	2 MHz / 256 MHz
Full scale	2.8 V_{p-p}	2.8 V_{p-p}
DR	81 dB	82 dB
SNR/SNDR	79.5 dB / 73.7 dB	80.5 dB / 74.4 dB
Power consumption	6.8 mW	5 mW
Active area	0.42 mm^2	0.33 mm^2
Inband IIP_3/IIP_2 (2MHz input tones)	22.3 dBFS / 73.5 dBFS	25.5 dBFS / 83 dBFS
Out-of-band IIP_3 (4.75 & 10.5MHz tones)	26.2 dBFS	35.7 dBFS

Performance comparison

	This work Upfront Filter H_1-ΔΣ	This work Embedded Filter Δ-H_1-Σ	Philips et al. ISSCC 2004	Munoz et al. ISSCC 2005	Sosio et al. ESSCIRC 2011
BW (MHz)	2	2	1	1	6
fs (MHz)	256	256	64	64	405
DR (dB)	81	82	65	71	75.6
SNDRmax (dB)	73.7	74.4	59	68.5	74.6
P_d (mW)	6.8	5	2	2.35	54
FoM_{SNDR} (fJ/lvl)	429.6	291.4	1373.1	540.4	1025.3
DR + $10\log_{10}(BW/P_d)$	165.7	168.0	152.0	157.3	156.1
Out-of-band IIP_3 (dBFS) 4.75 & 10.5 MHz tones	26.2	35.7	5.7	-	-
(Filter 3dB BW)/Signal BW	2	2	3	-	1.43
Active area (mm^2)	0.42	0.33	0.14	0.1	0.21
Technology (nm)	130	130	180	180	90

Conclusions

- Embedding a filter inside a CTDSM
  - More power efficient and linear
  - Loop stabilized without extra hardware

- 2^{nd} order filter inside a 4^{th} order CTDSM
  - Compared to filtering upfront
    - Better out-of-band IIP_3
    - Better inband IIP_3 / IIP_2
    - Lower power consumption and active area

Acknowledgement

- Department of Science and Technology, Government of India
  - For funding
- Europractice
  - For chip fabrication
- Dr. N. Krishnapura and Dr. S. Aniruddhan
  - For useful discussions

A 235mW CT 0-3 MASH ADC achieving −167dBFS/Hz NSD with 53MHz BW

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[1]Analog Devices, Toronto, ON, Canada
[2]Analog Devices, Wilmington, MA, United States
[3]University of Toronto, Toronto, ON, Canada

Outline

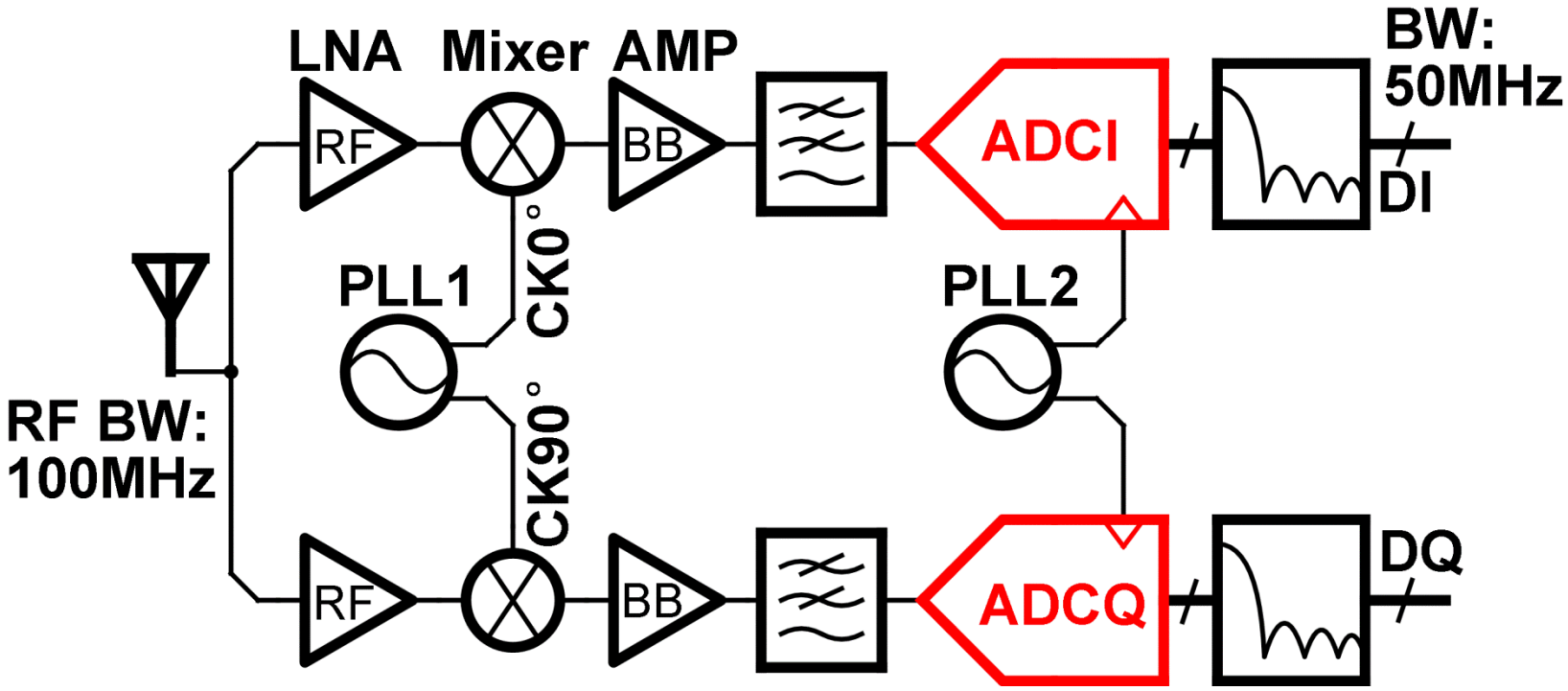
Motivation

A CT 0-3 MASH ADC in 28nm CMOS

- ADC Architecture
- Circuit Building Blocks
  - Third-order Feedforward Amplifier
  - Complementary Current DAC
  - Comparator with Boosted Gm
- Experimental Results

Summary

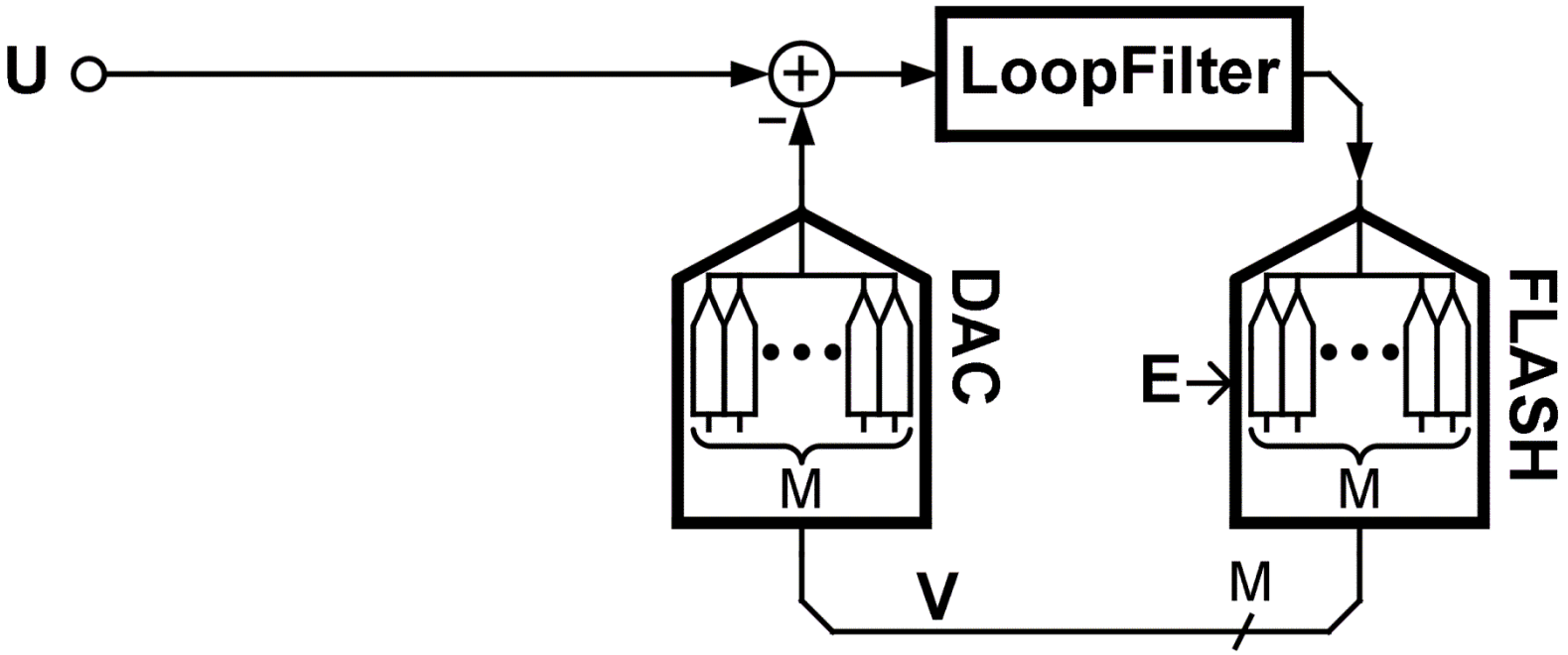
Motivation



LTE-A direct-conversion receiver: 100MHz RF BW

ADC: 50MHz BW, low power (<0.25W), high DR (>80dB)

A Continuous-Time FF ΔΣ ADC?

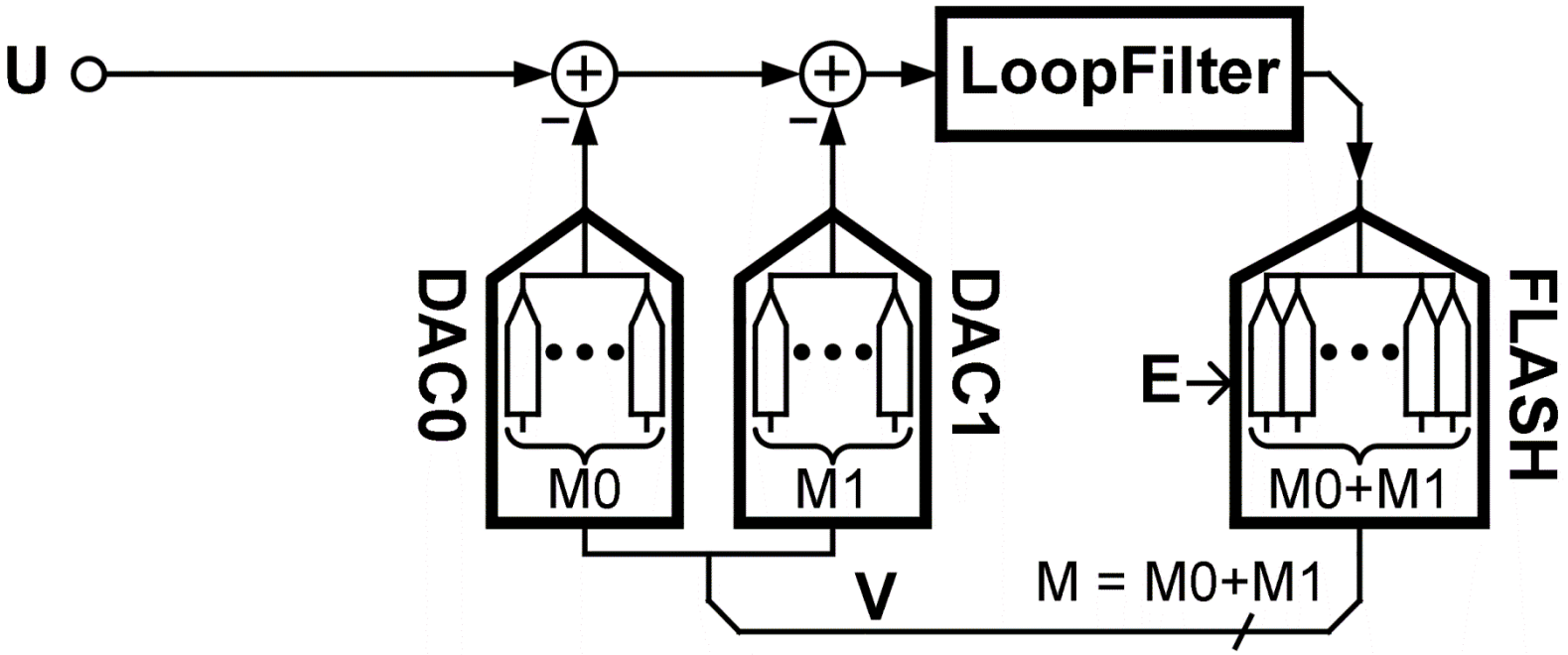


V = U*STF + E*NTF

Very power-efficient architecture ☺

Peaking STF: hurts blocker tolerance ☹

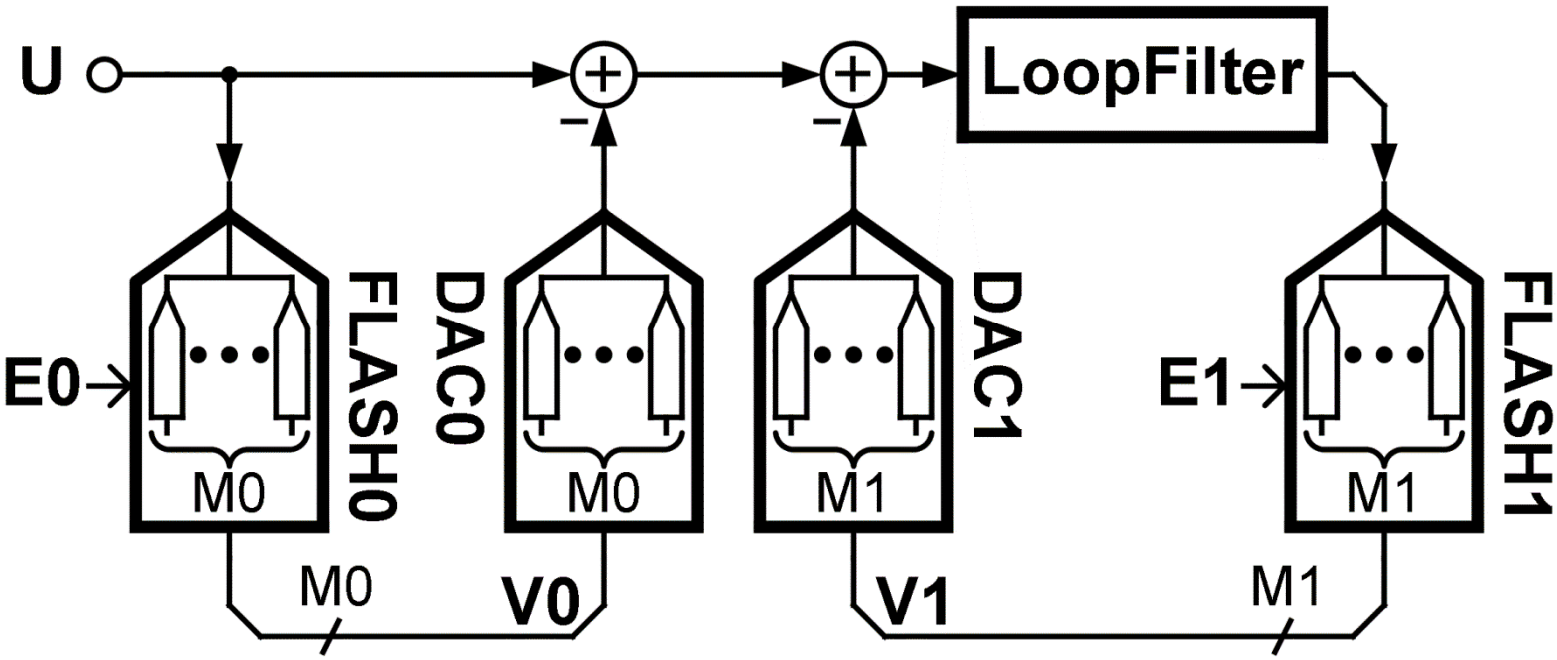
Splitting the DAC



M = M0 + M1

DAC → DAC0 & DAC1

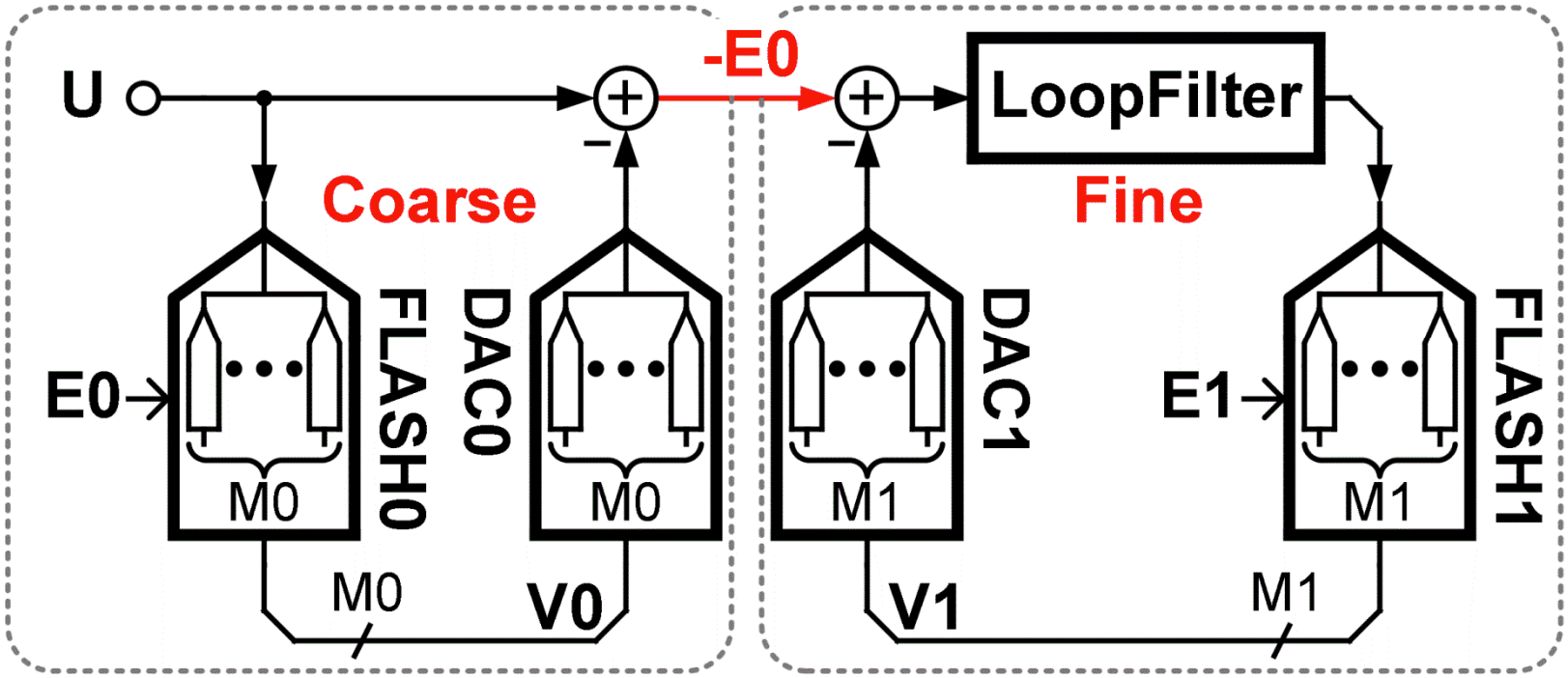
Splitting the FLASH



M = M0 + M1

FLASH → FLASH0 & FLASH1

A CT 0-X FF MASH ADC



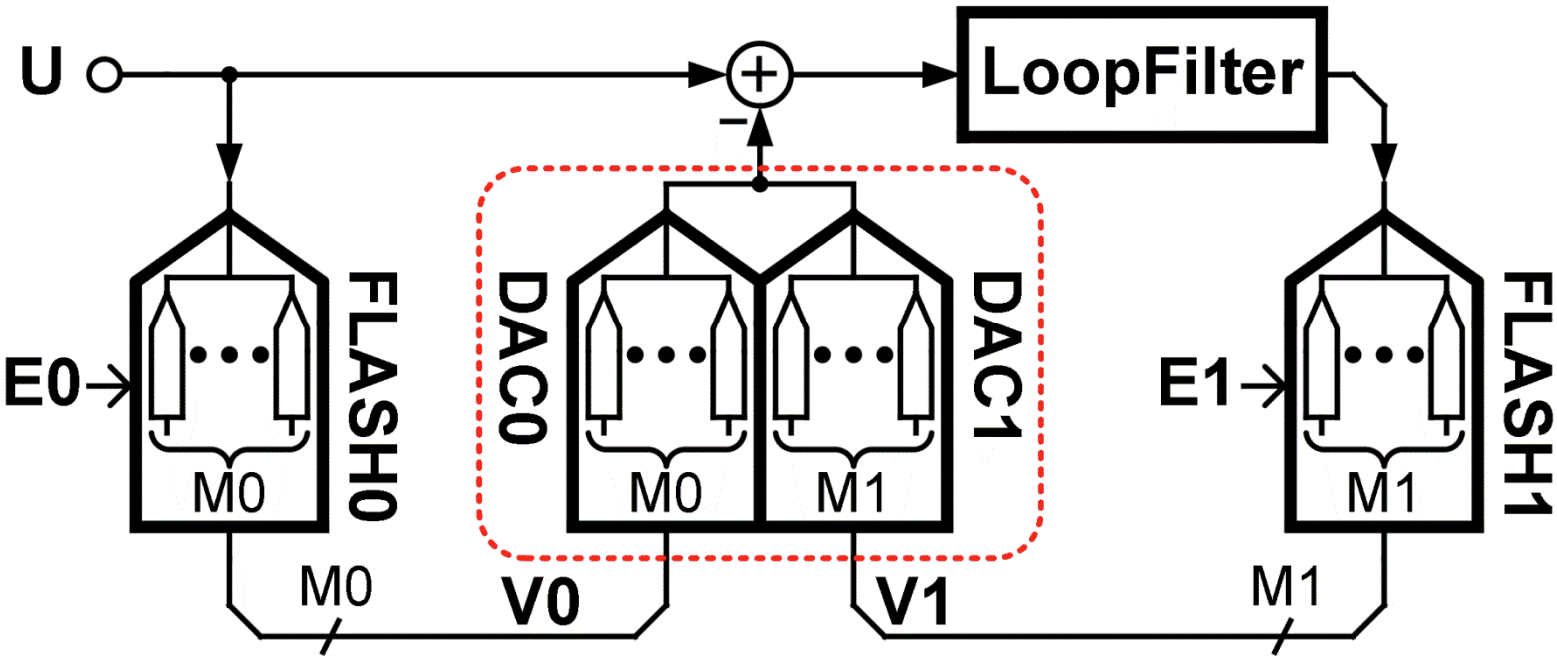
A. Gharbiya, et al, *JSSC*. 2009, N. Maghari, et al, *JSSC*. 2009

V0 = U + E0

V1 = (-E0)*STF + E1*NTF

V1 = (-E0)*(1 - NTF) + E1*NTF

A CT 0-X FF MASH ADC



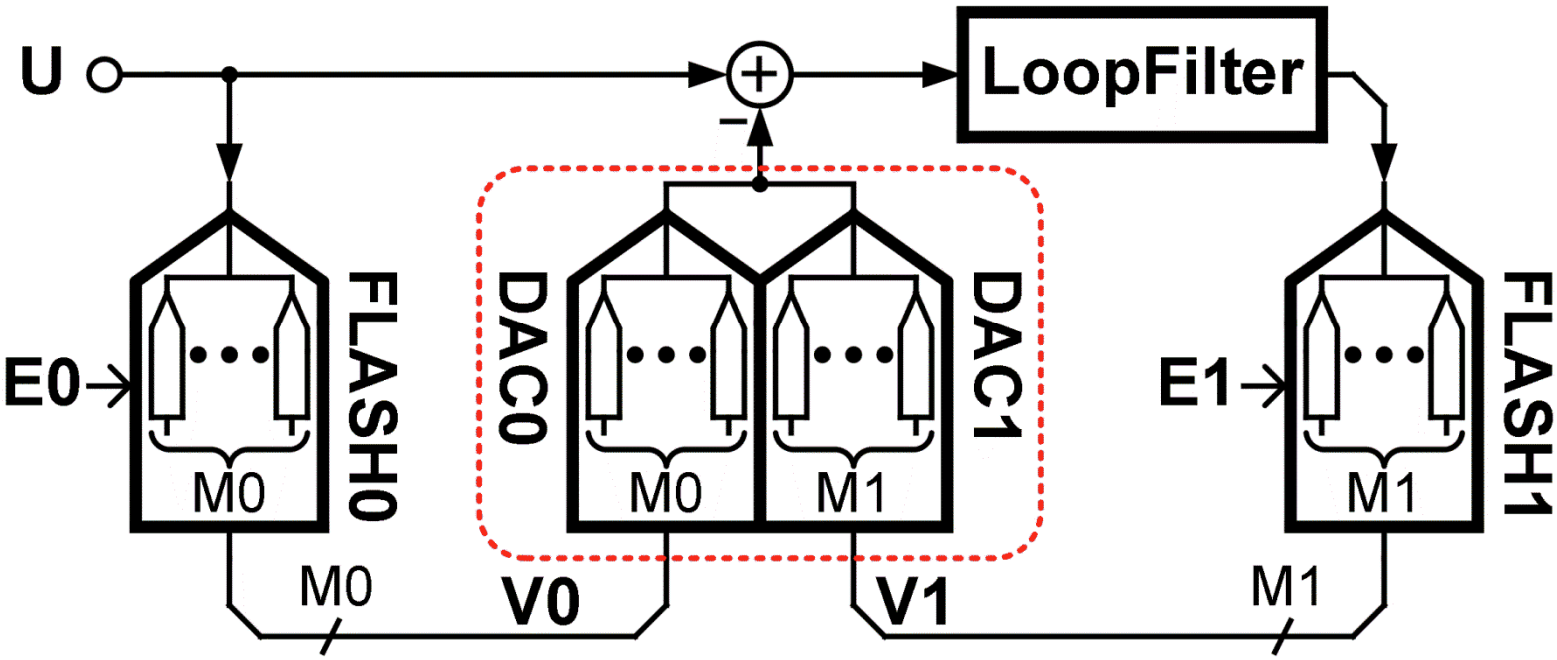
A. Gharbiya, et al, *JSSC*. 2009, N. Maghari, et al, *JSSC*. 2009

V = V0 + V1 = U + (E0 + E1)*NTF

Flat STF: improved blocker tolerance ☺

Adding E0, hurts quantization noise ☹

Noise Cancelling in 0-X MASH

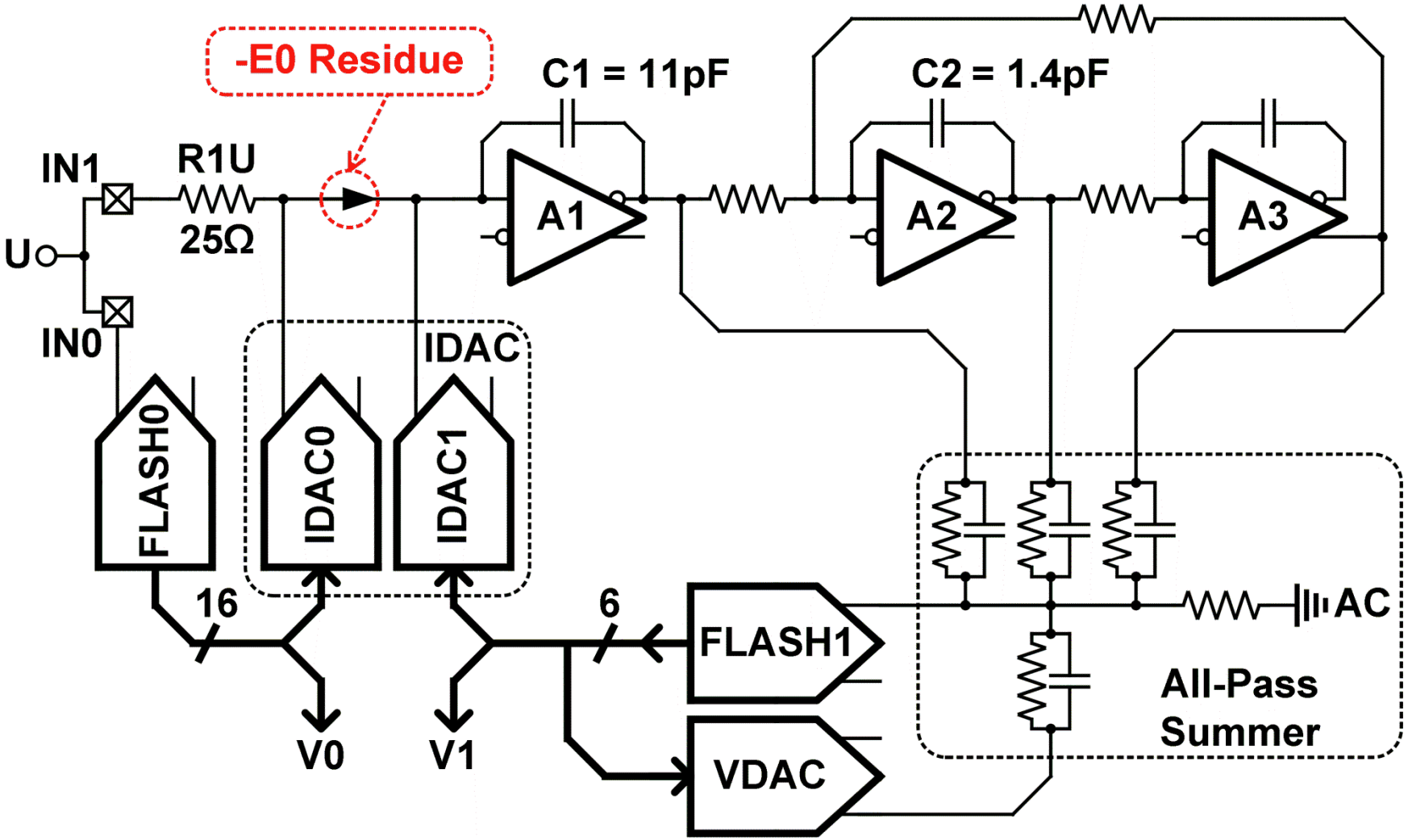


V = V0 + V1*1/STF = U + E1*NTF/STF

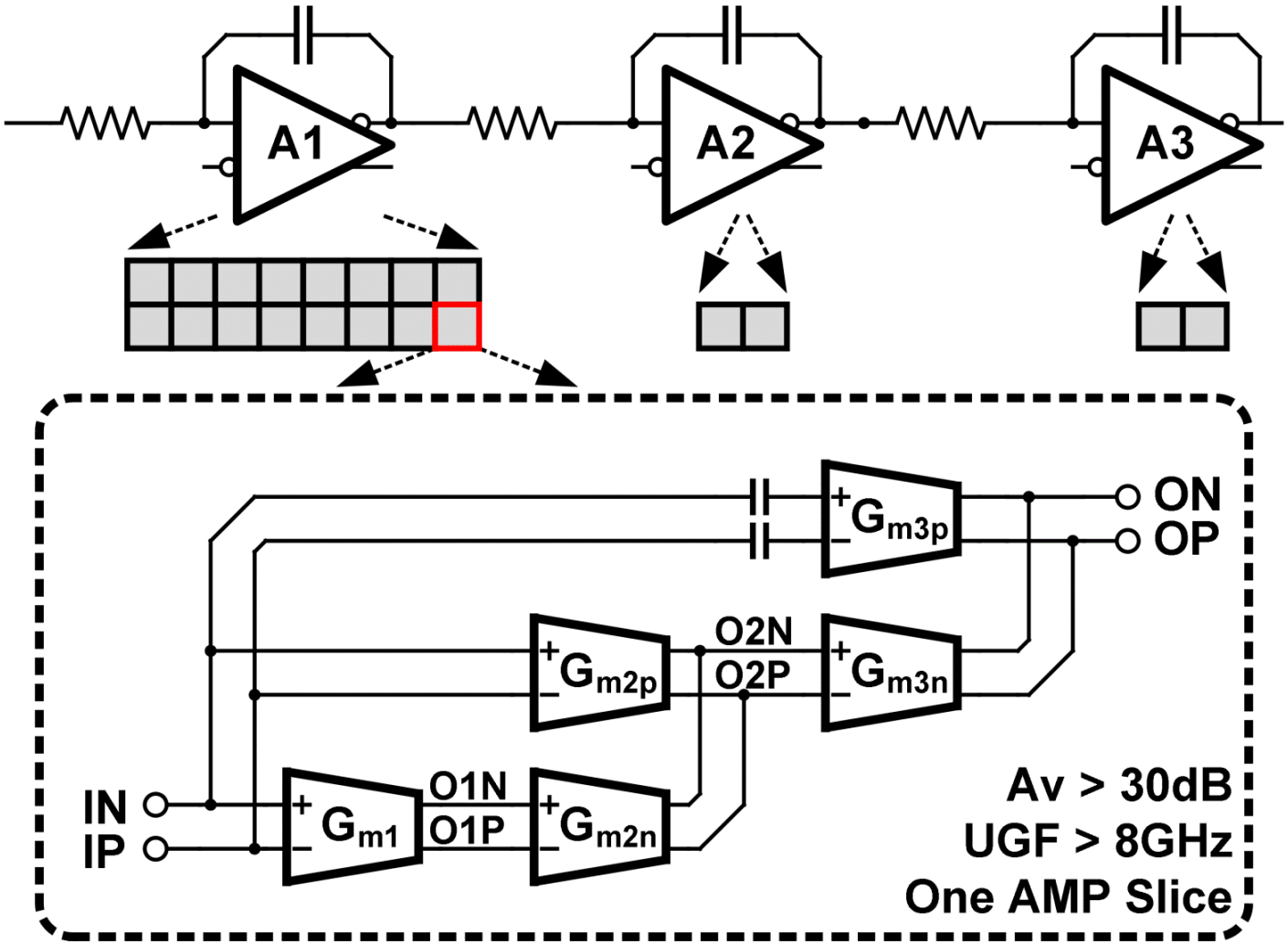
Eliminates E0 added by FLASH0 ☺

Easy match STF between Analog & Digital ☺

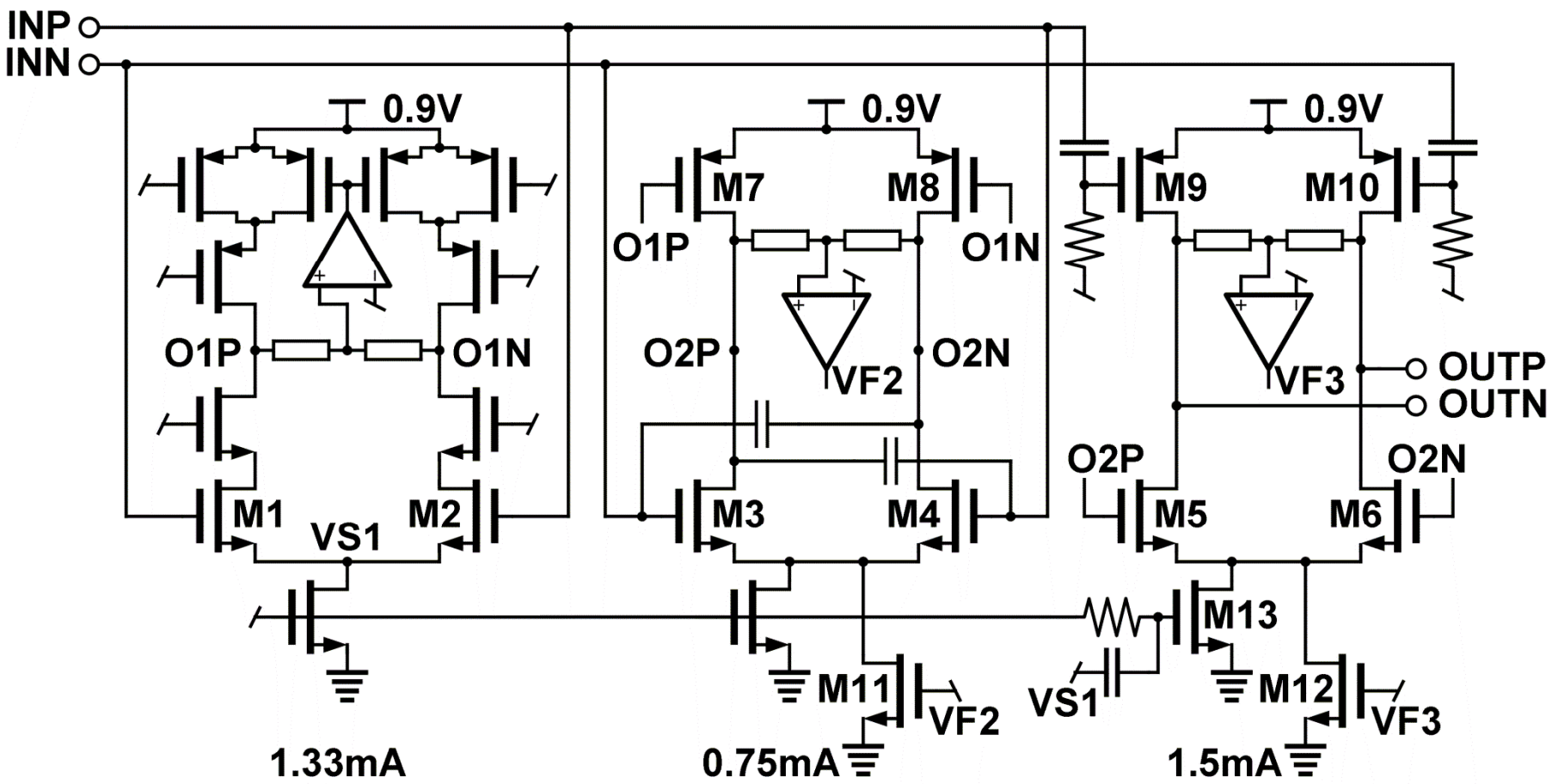
A CT 0-3 FF MASH ADC



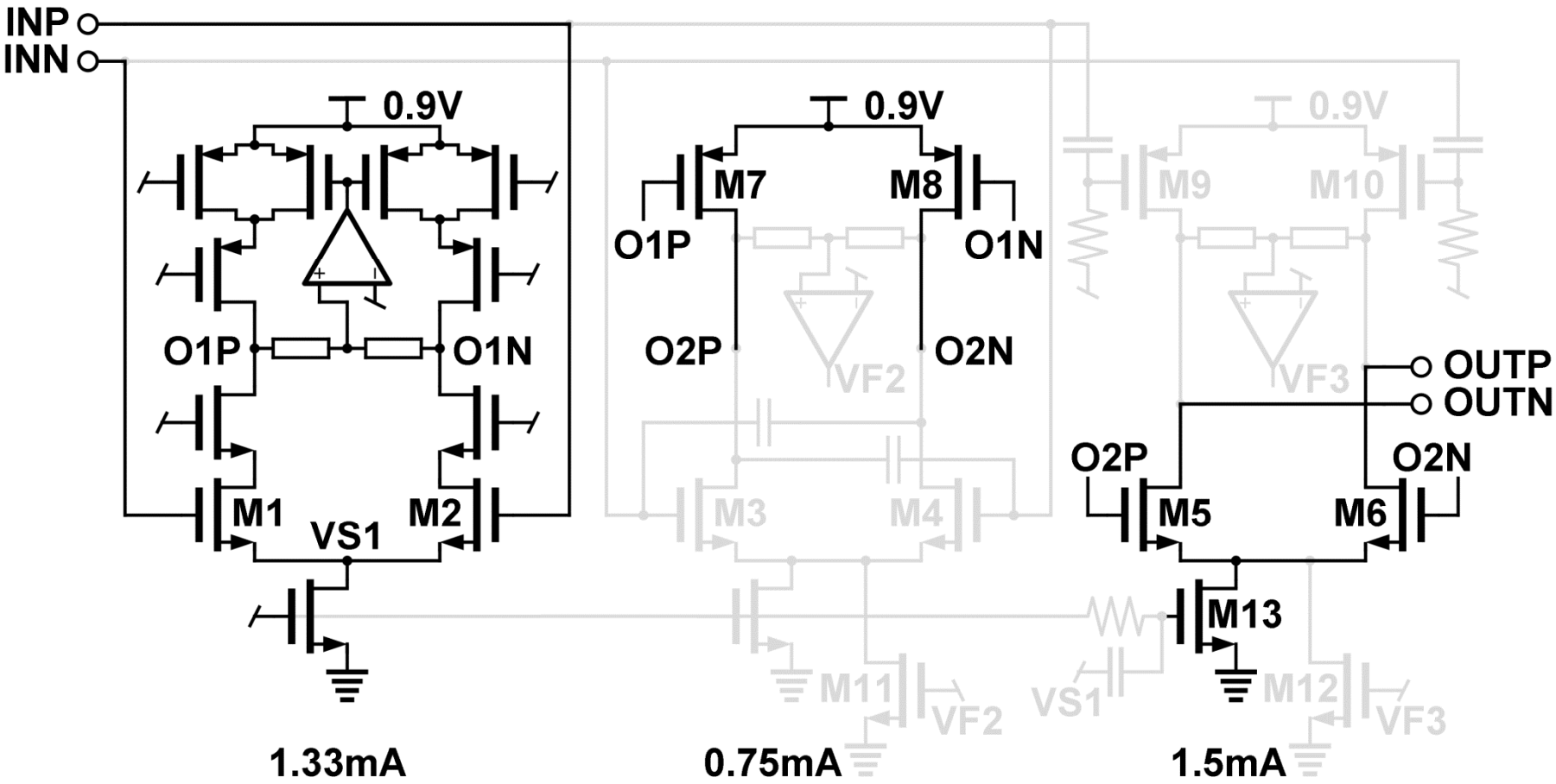
3rd-order Feedforward AMP



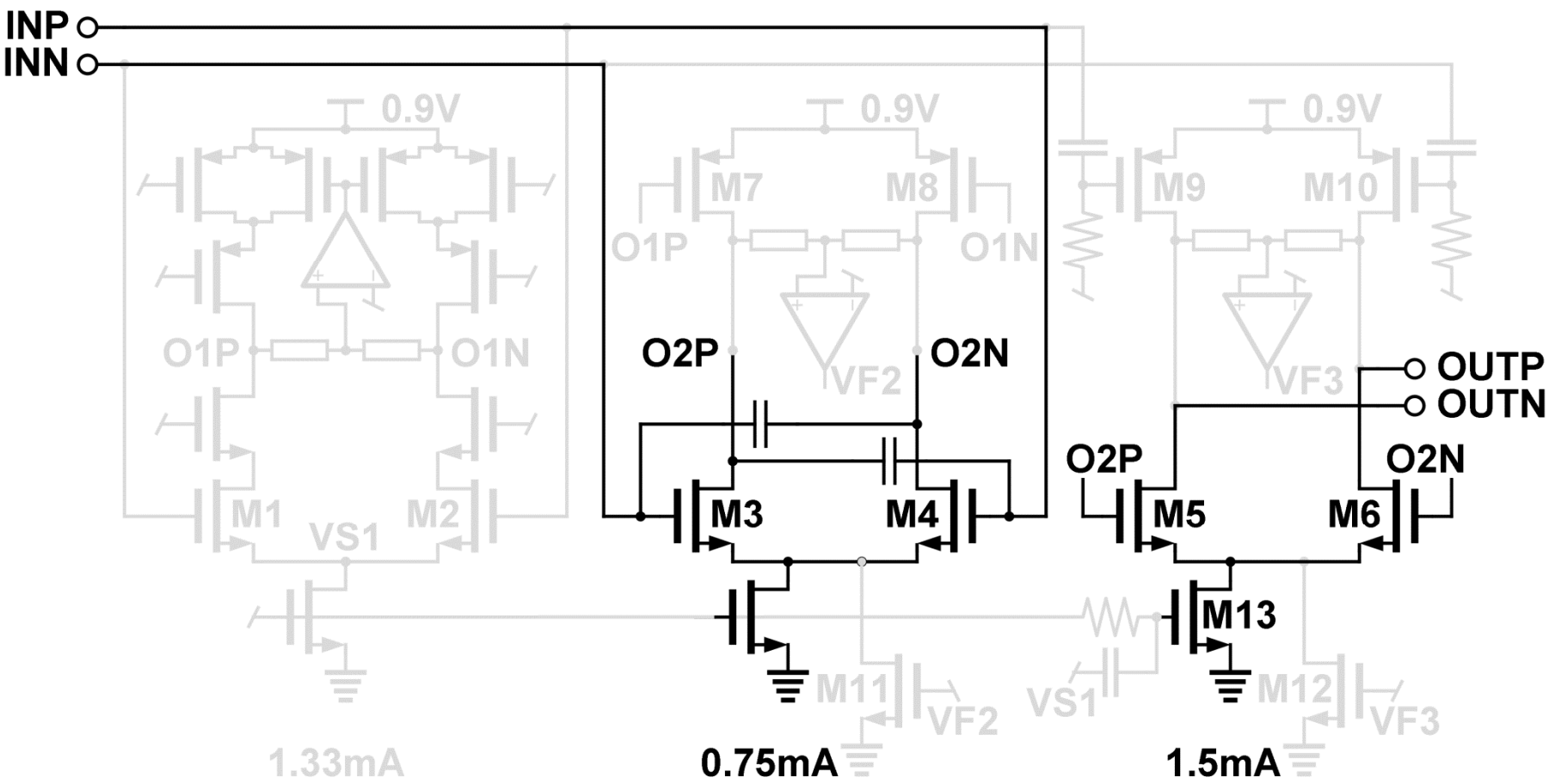
One Slice of FF-AMP



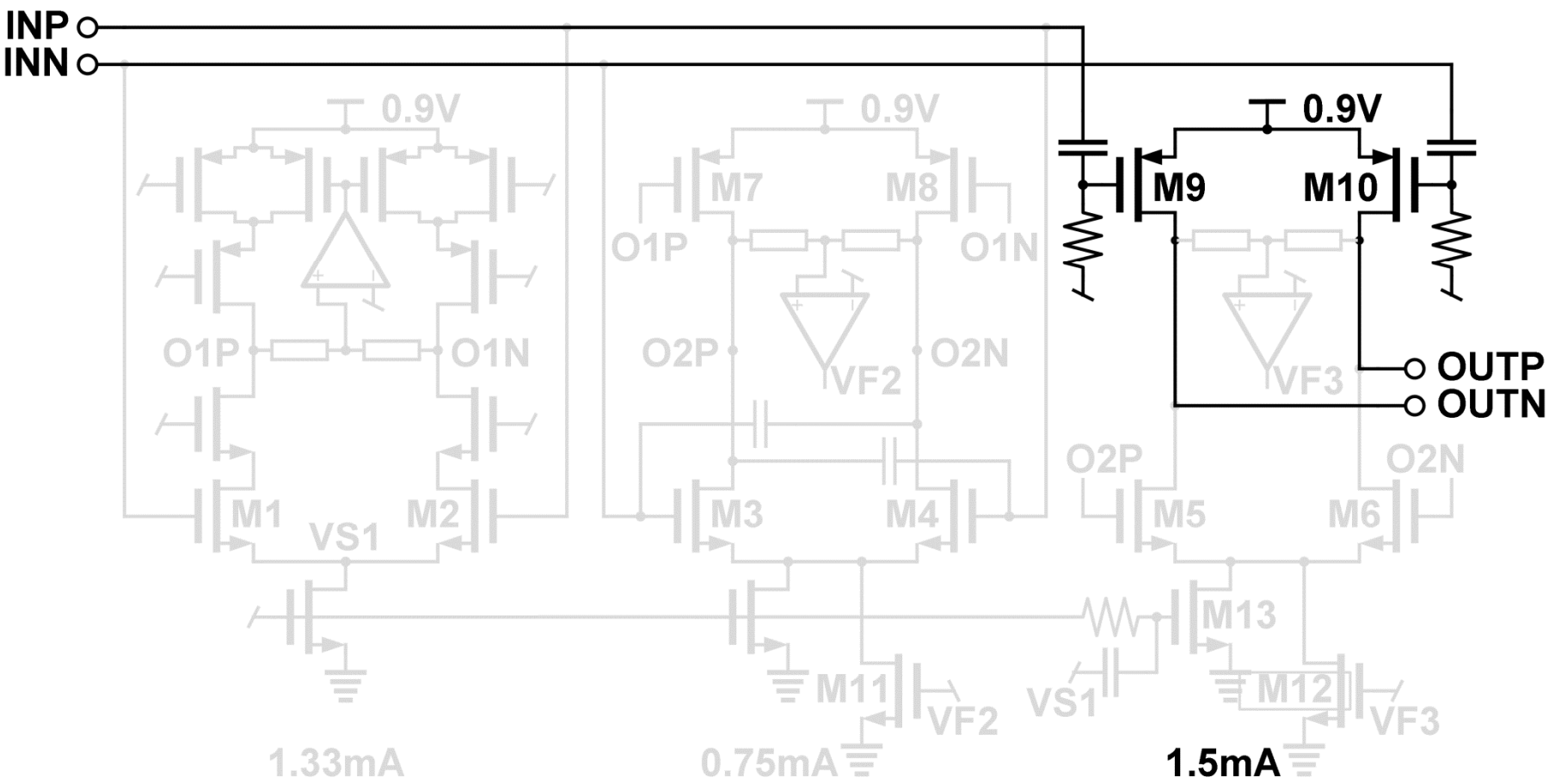
Third-order Gain Path



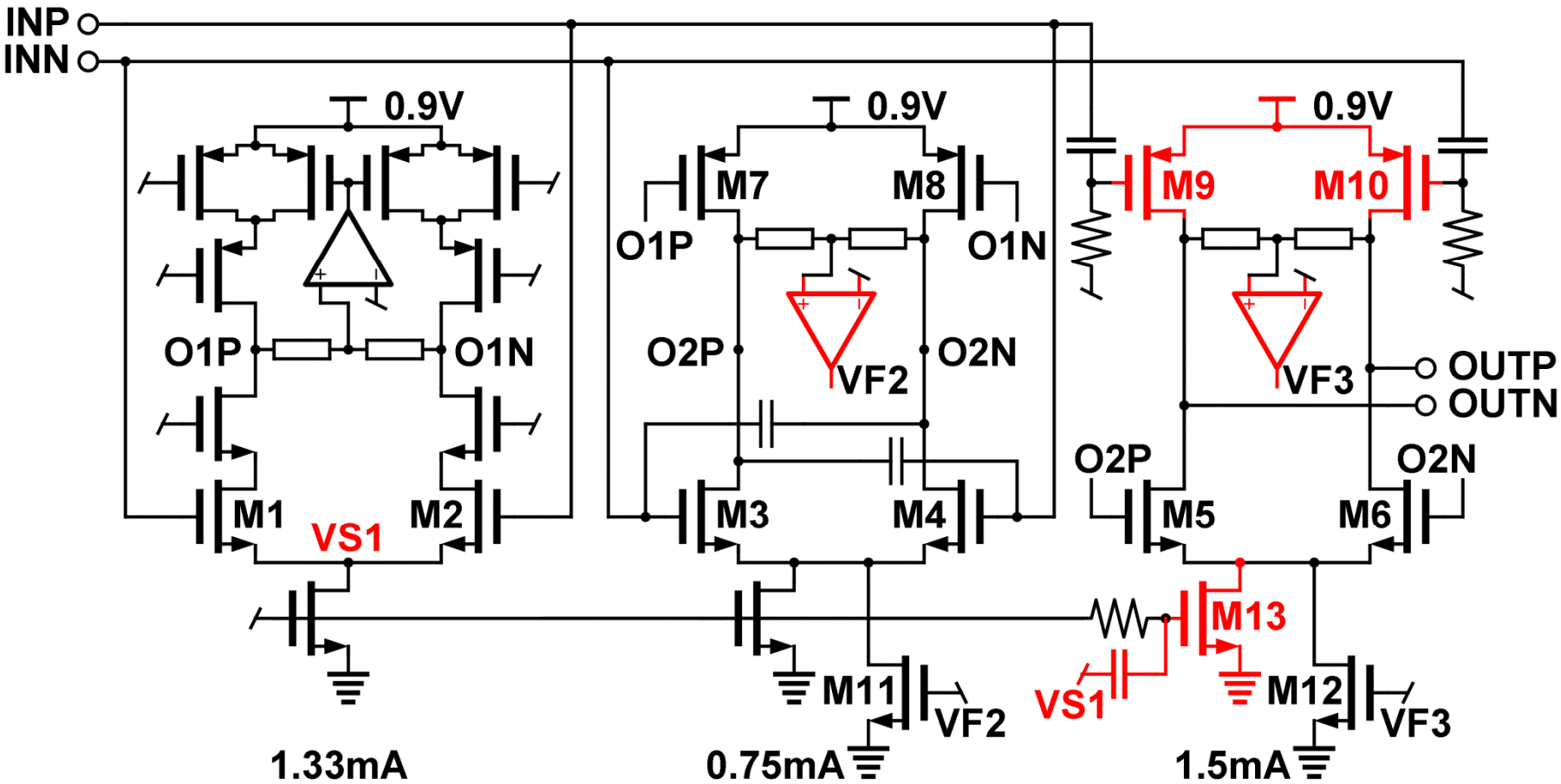
Second-order Gain Path



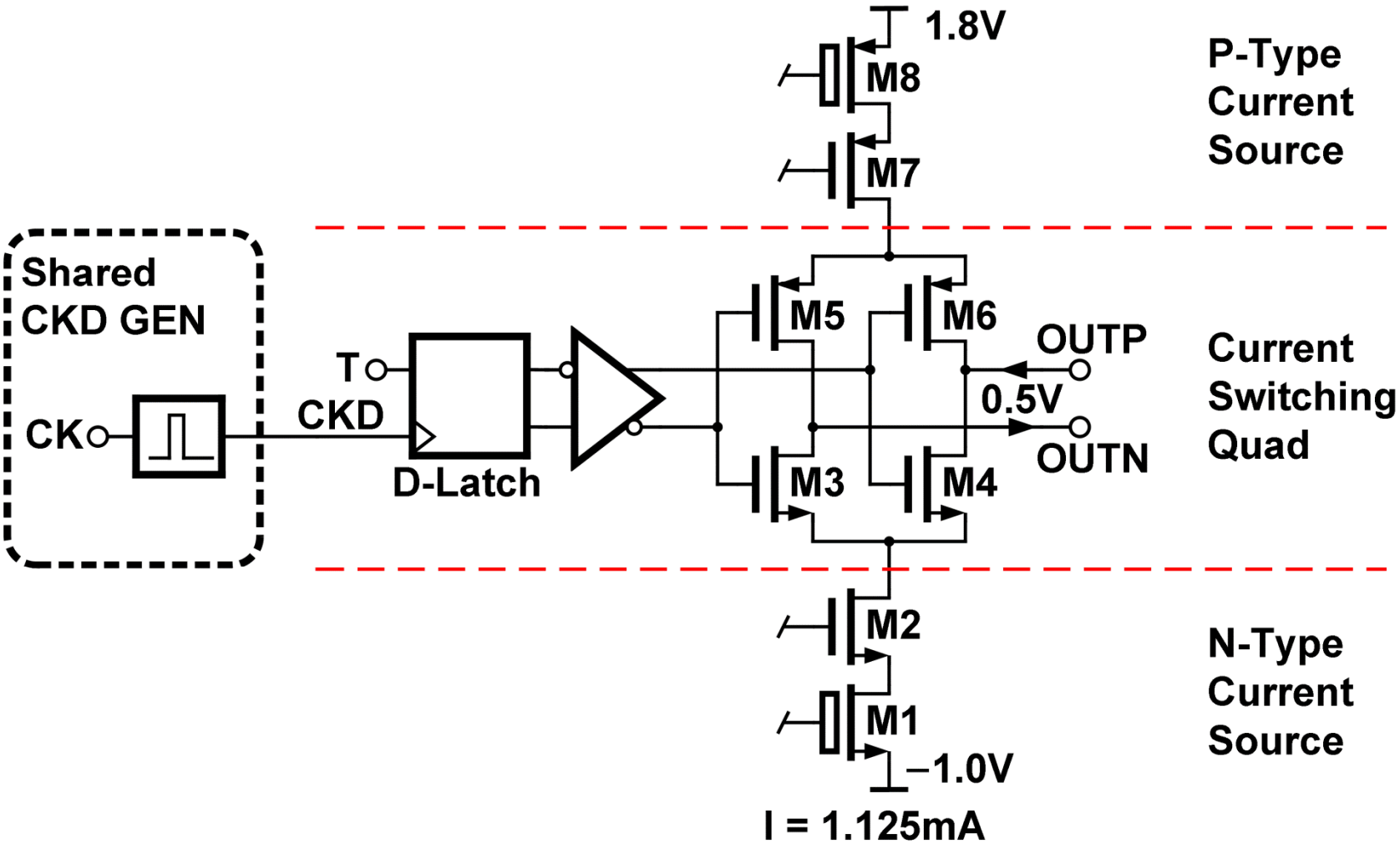
First-order Gain Path



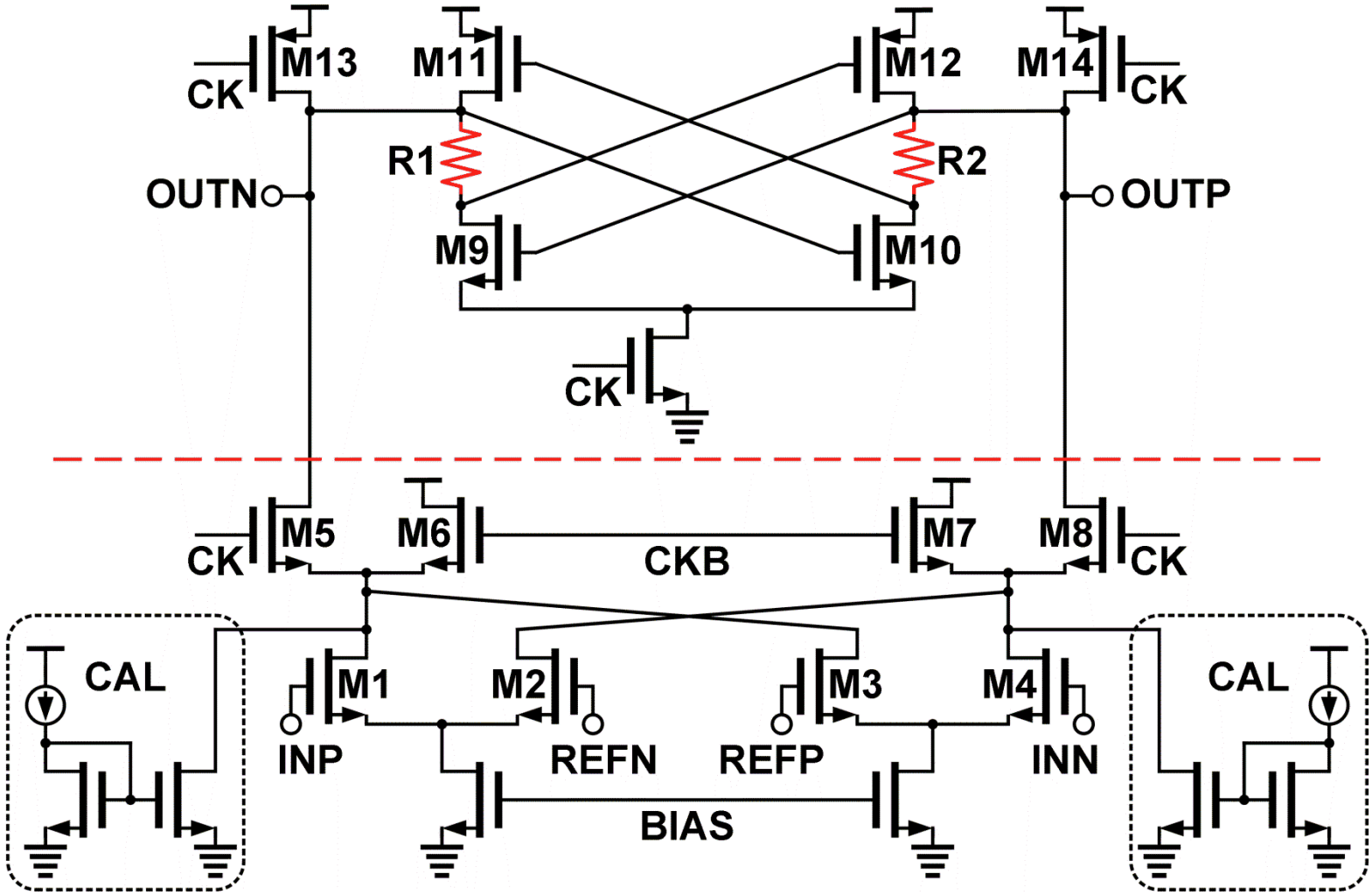
Common-mode Stabilization



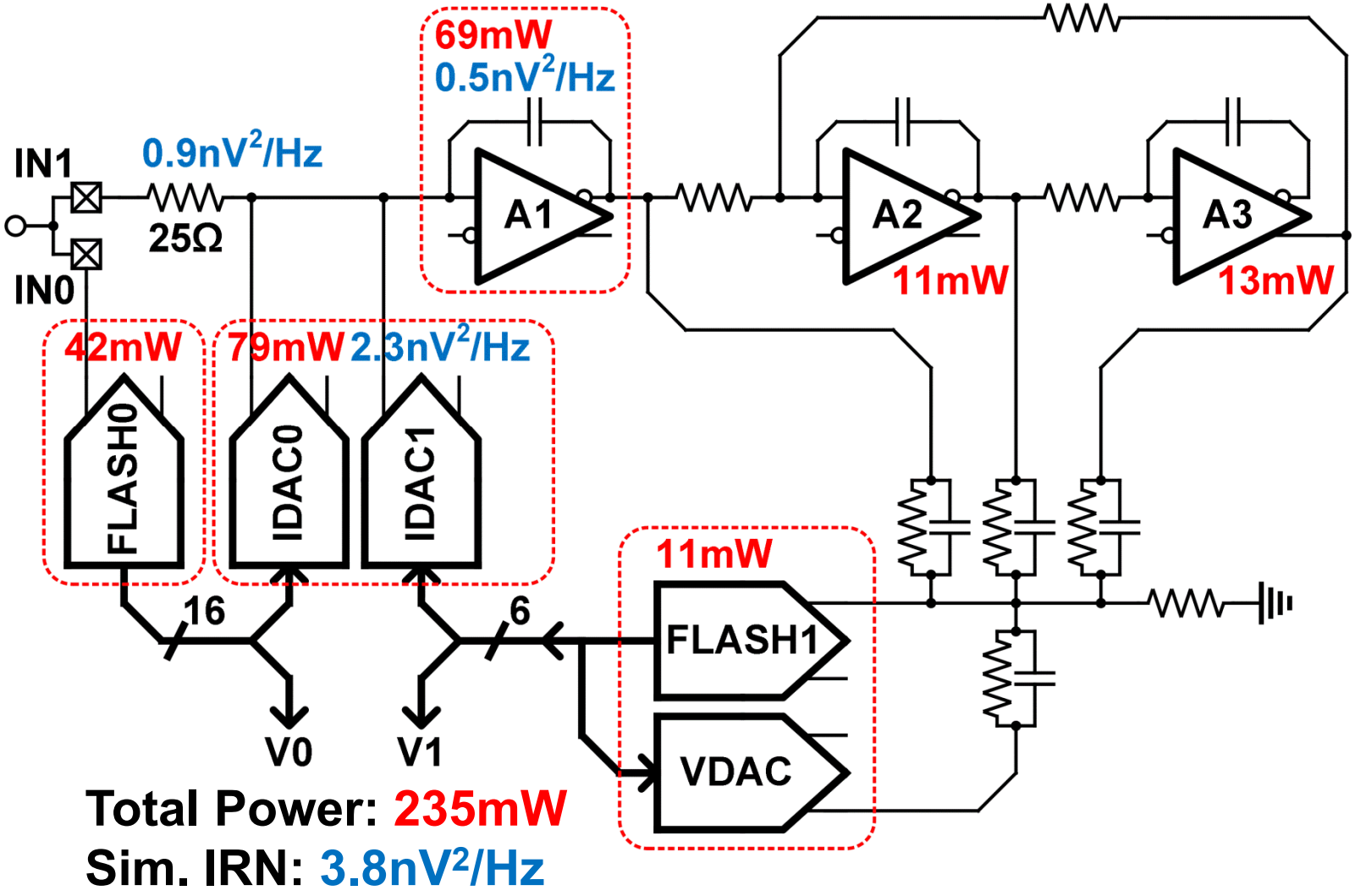
Complementary IDAC Cell



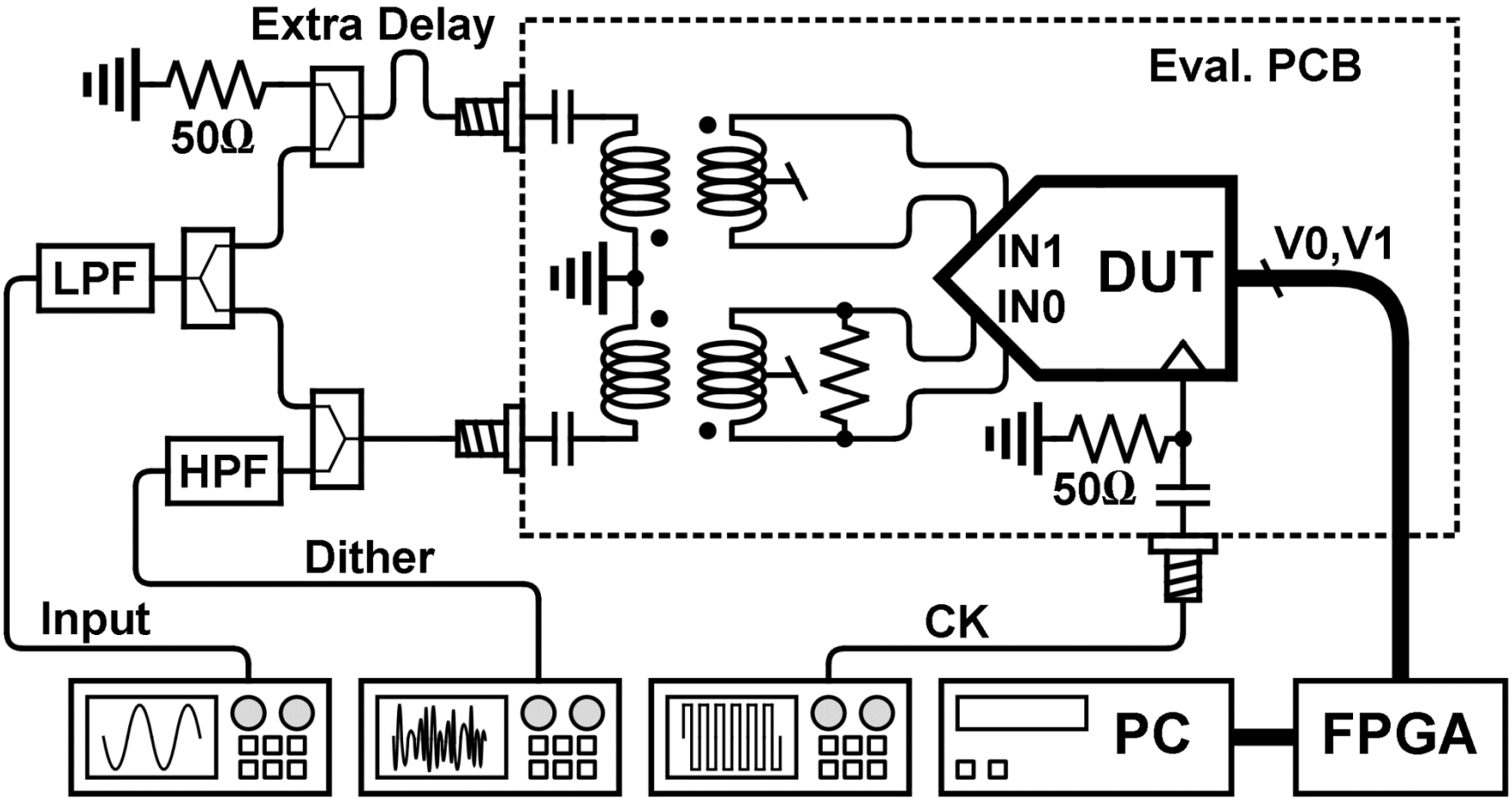
FLASH Comparator



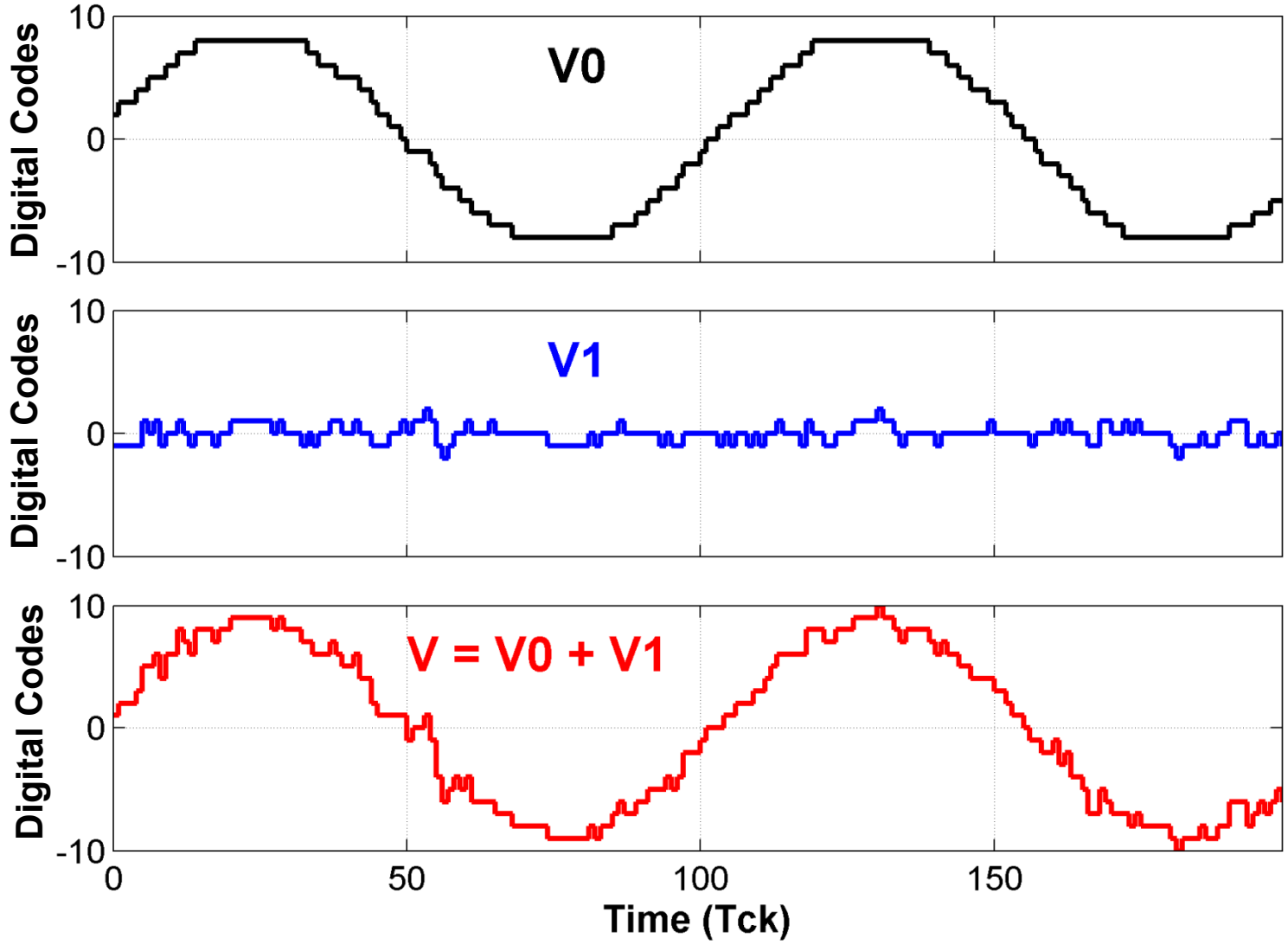
Power Consumption



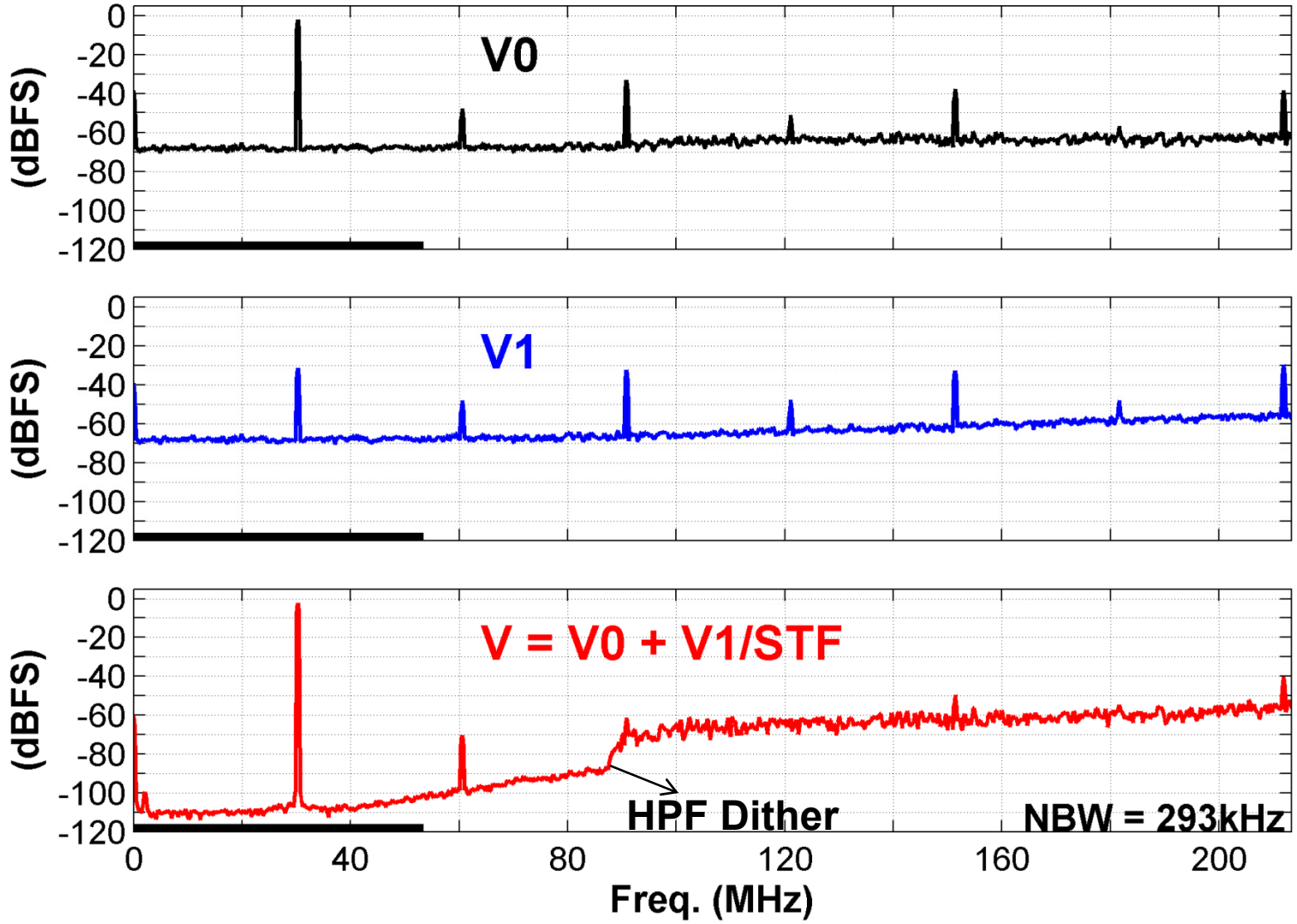
Measurement Setup



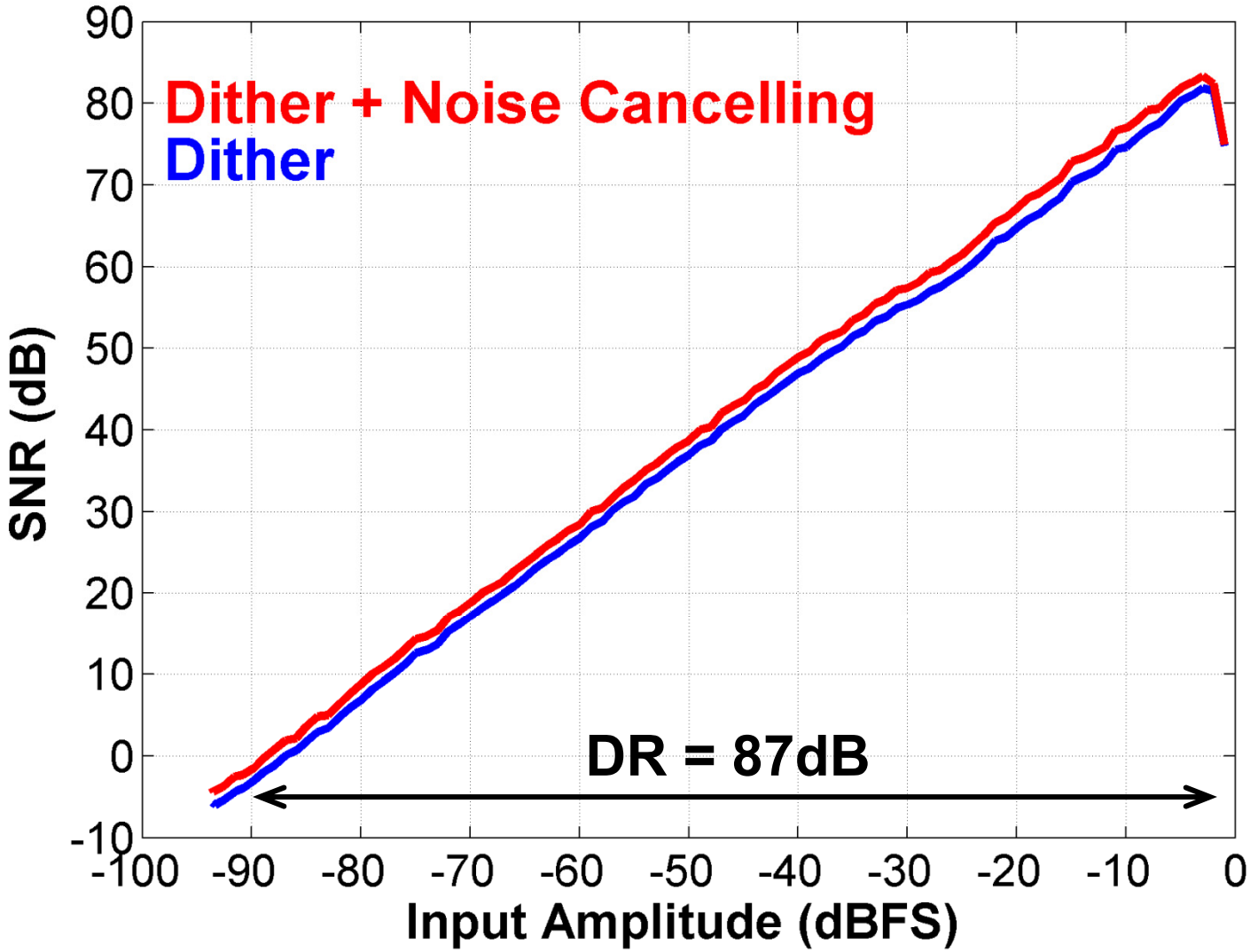
-2dBFS One Tone at 30MHz



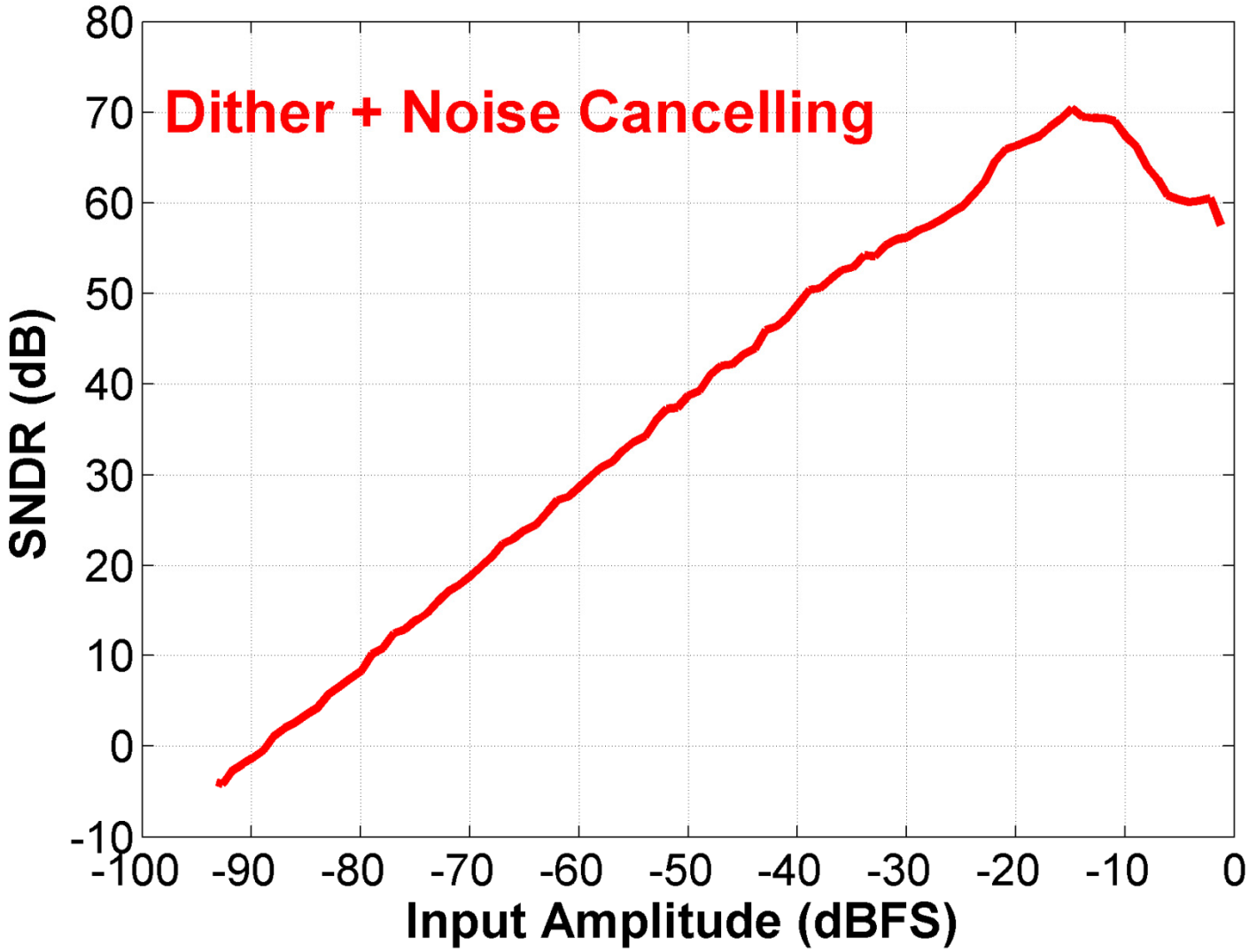
-2dBFS One Tone at 30MHz



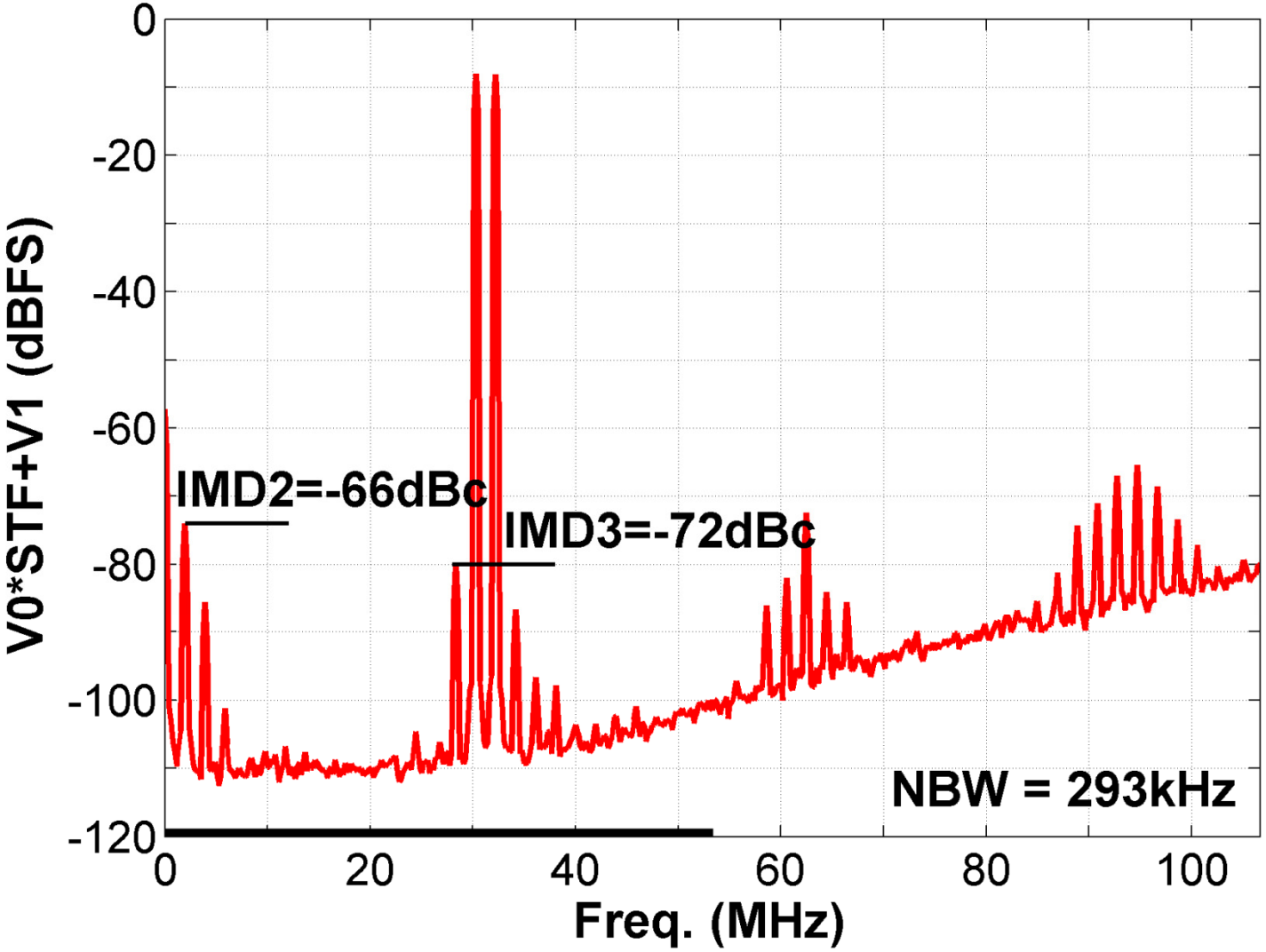
SNR vs. Input at 30MHz



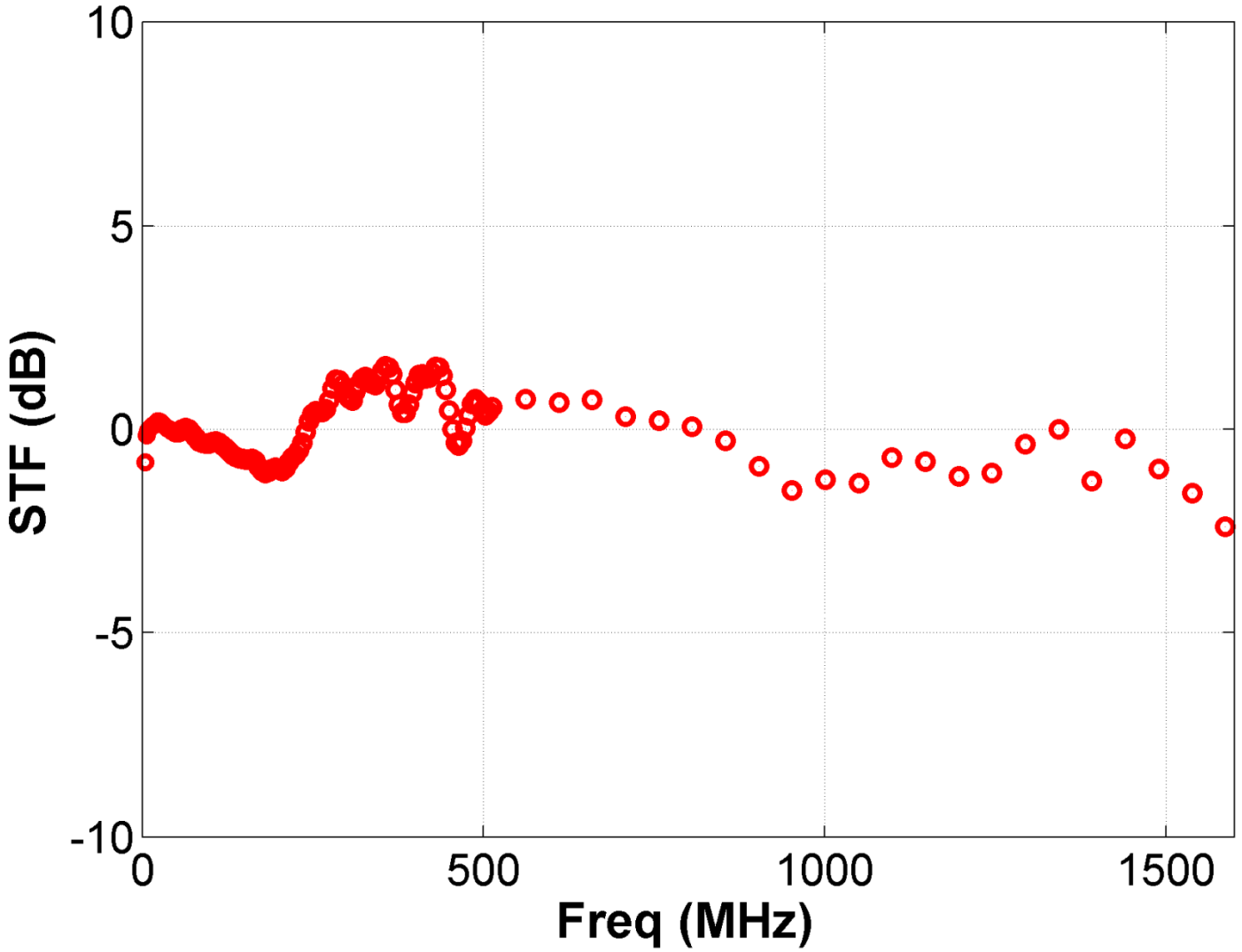
SNDR vs. Input at 15MHz



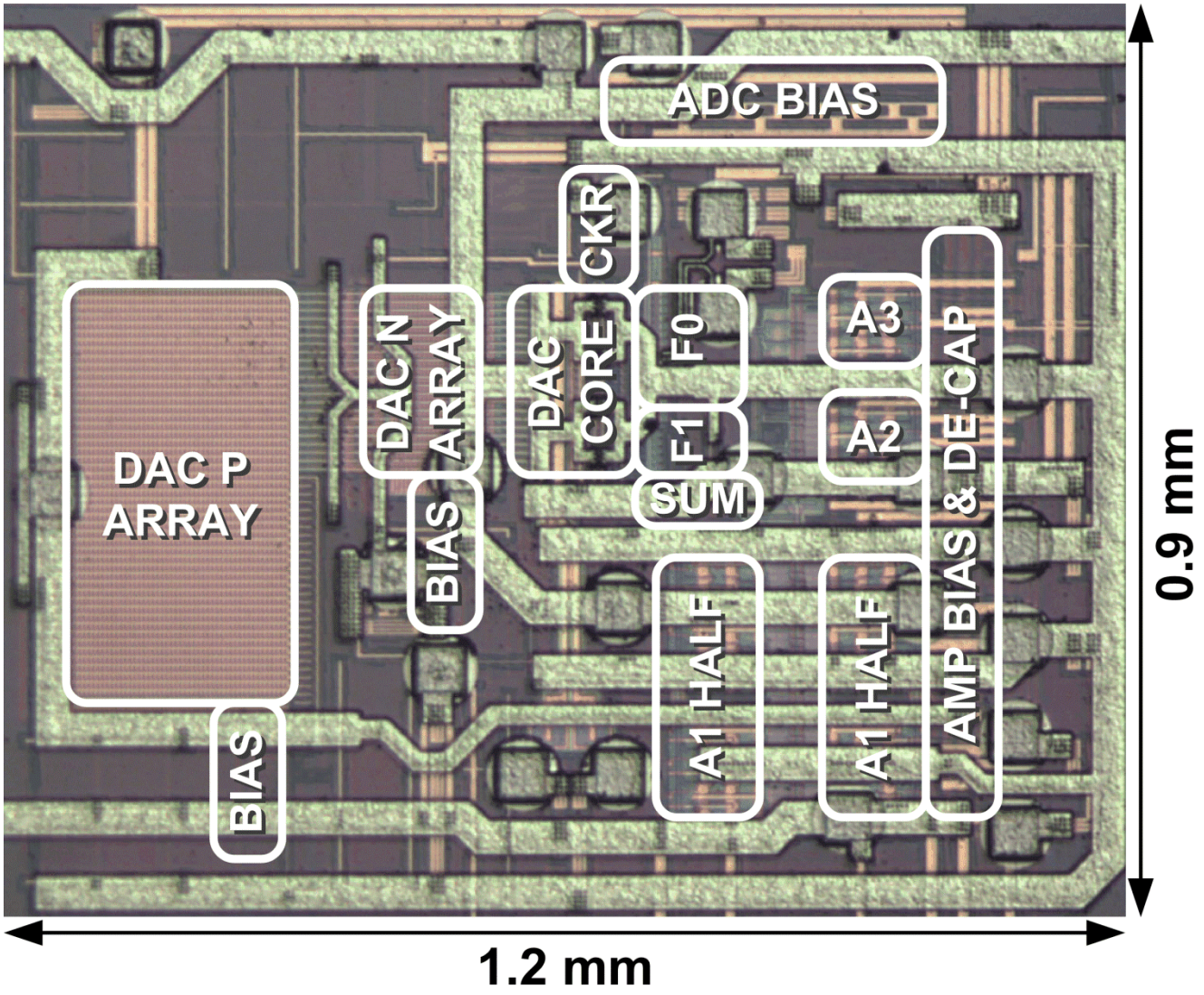
Spectra -8dBFS Two-Tone



Signal Transfer Function



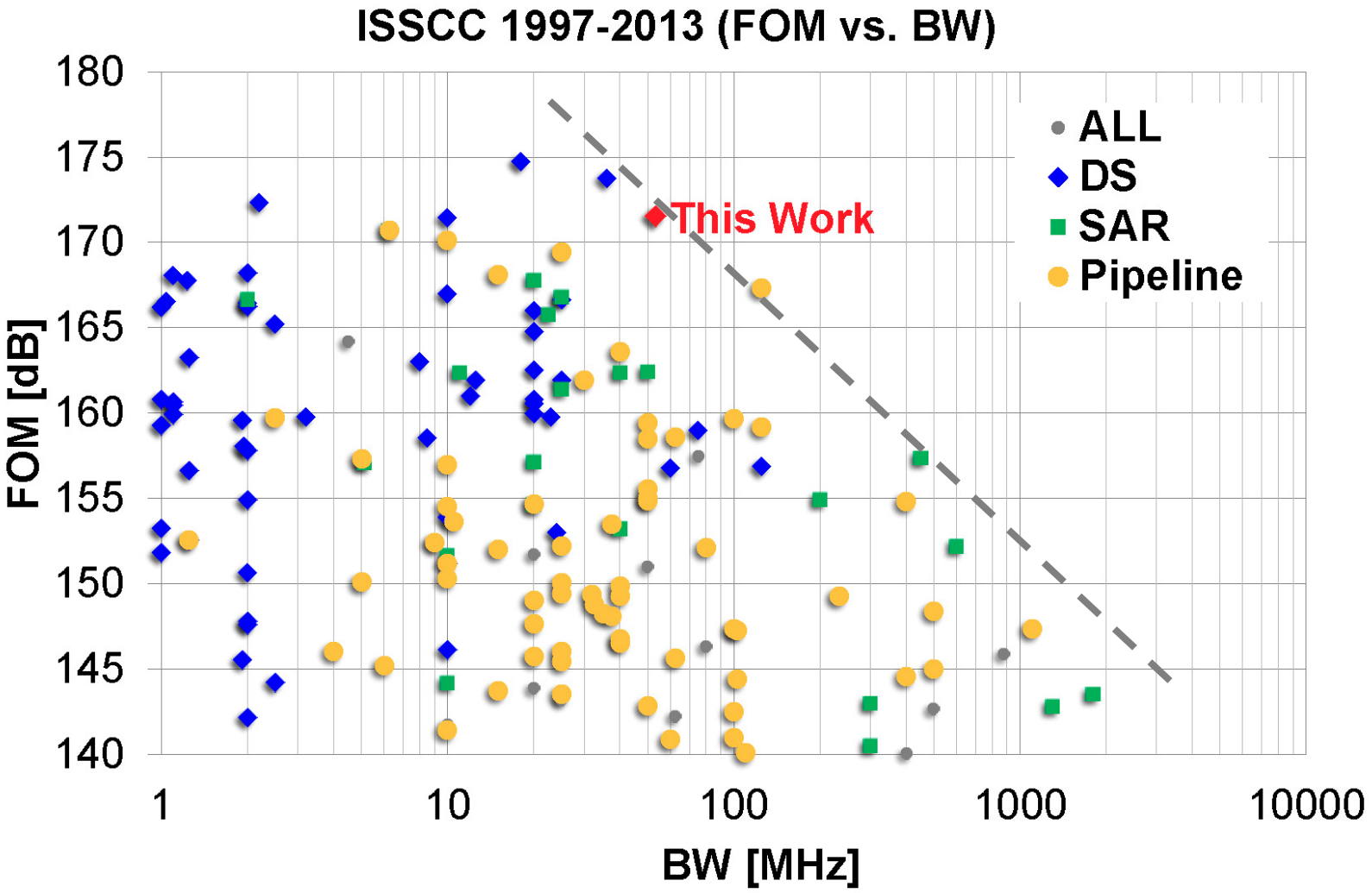
Die Microphotograph



Chip Summary

CMOS Technology	28nm HKMG Bulk CMOS	
Active Area	$0.9mm^2$	
Supply Voltages	0.9/1.8/–1.0V	
Power (P)	235mW	
Sampling Rate	3.2GHz	
Bandwidth (BW)	53MHz (OSR = 30)	
Input Full Scale	2.5V differential p-p	
Dither to FLASH0	NO	YES
Average NSD with Small Input Signal	3.9nV/rtHz (–167dBFS/Hz)	4.3nV/rtHz (-166dBFS/Hz)
Dynamic Range (DR)	88dB	87dB
Peak SNR	84.6dB	83.1dB
Peak SNDR	71.8dB	70.0dB
FOM = DR+10log$_{10}$(BW/P)	171.6dB	170.6dB

FOM VS. BW



Summary

CT 0-X FF MASH ADC

- Power efficiency of a CT FF ΔΣ ADC
- Flat STF → Better blocker tolerance
- Robust E0 Noise Cancellation

A 0-3 CT FF MASH ADC

- NSD of -167dBFS/Hz with 235mW
- DR of 88dB & FOM of 171.6dB over 53MHz

Acknowledgements

Ziwei Zheng for digital design;

Chuanwei (Jason) Li, Kevin Lam, Bill Harrington for excellent layout work;

Anthony Del Muro, Abrar Ahmed Pathan for their help in the lab;

Bob McLeod for taking the die photo;

The Analog Devices CAD team and HSC for their advice, encouragement and support;

A 14b 1GS/s RF Sampling Pipelined ADC with Background Calibration

Ahmed M.A. Ali, Huseyin Dinc, Paritosh Bhoraskar, Chris Dillon, Scott Puckett, Bryce Gray, Carroll Speir, Jonathan Lanford, David Jarman, Janet Brunsilius, Peter Derounian, Brad Jeffries, Ushma Mehta, Matt McShea and Ho-Young Lee

Analog Devices, Inc.

Outline

- Architecture
- Circuit design techniques
- Background Calibration
  - Inter-stage Gain Errors (IGE: Static and Dynamic)
  - Inter-stage Memory Errors (IME: Static and Dynamic)
  - Input Kick-Back Calibration
- Silicon results
- Conclusion

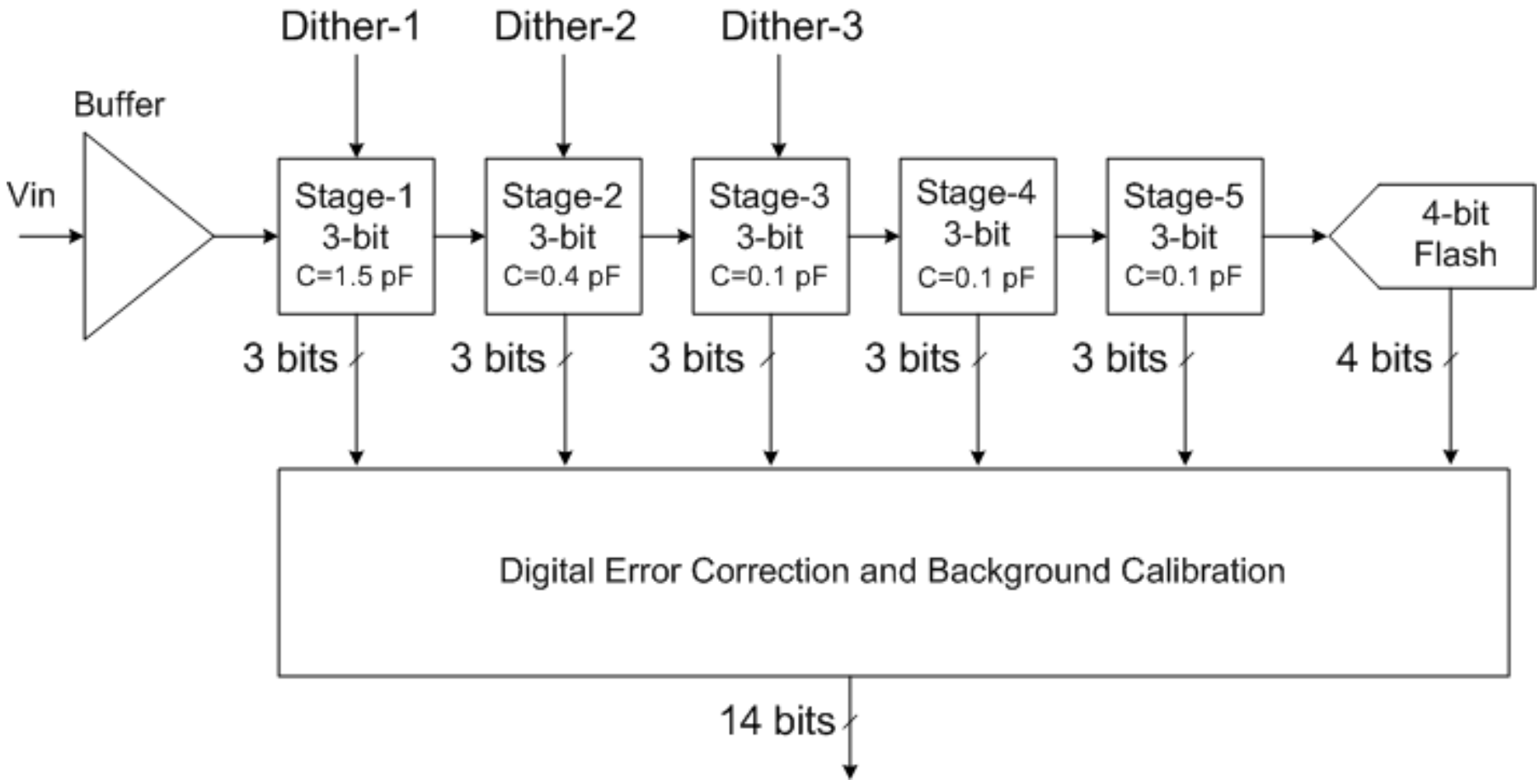
Objectives

- Sample rate of 1GS/s:
  - Enables higher bandwidth
  - Simplifies anti-aliasing filter
  - Achieves oversampling processing gain
- Noise density (-153dBFS/Hz to -156dBFS/Hz)
- RF sampling: Good linearity SFDR > 80dB up to 1GHz input frequency
- Full Nyquist BW operation

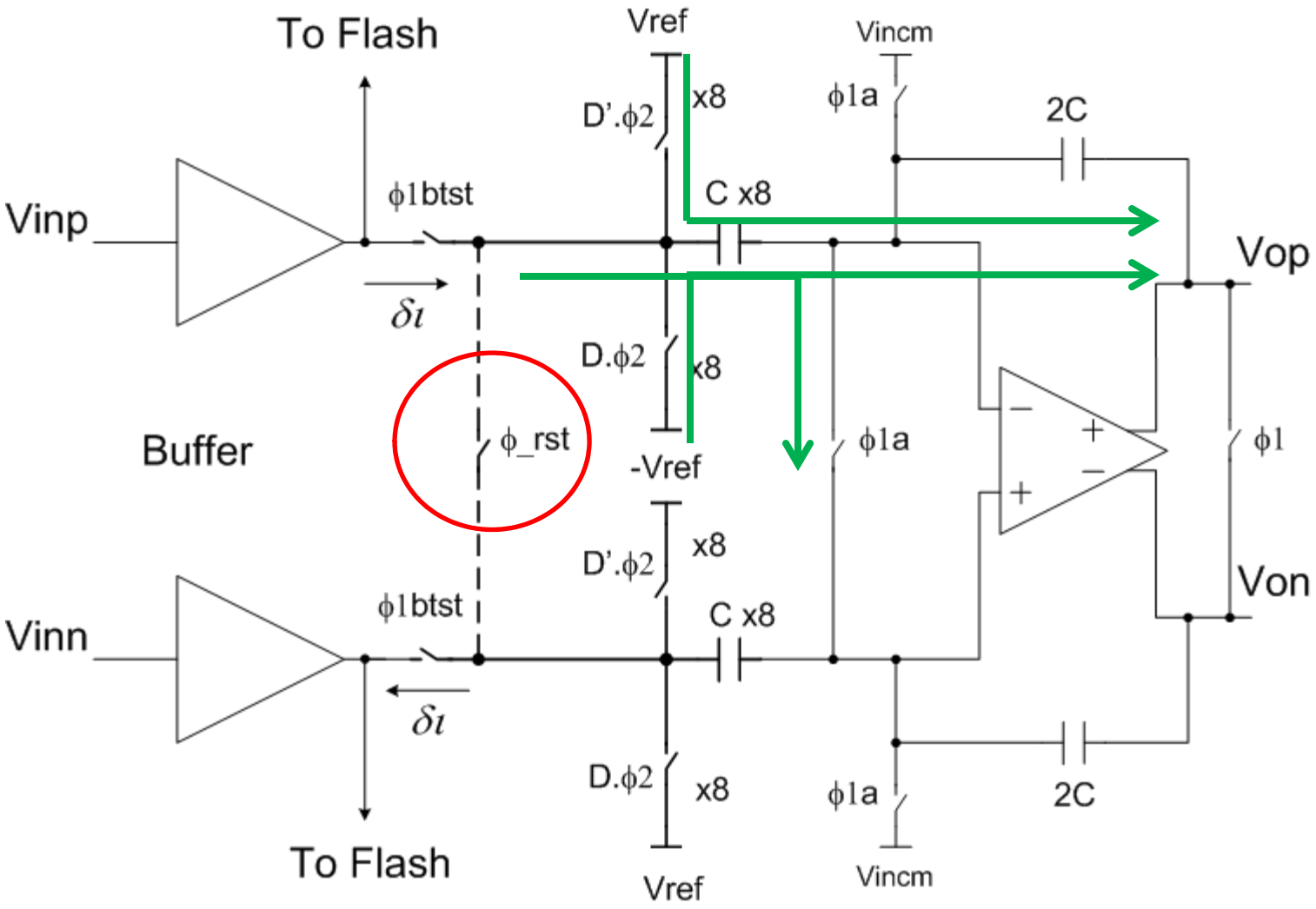
Design Challenges

- High sample rate + Performance SFDR/SNR
- No interleaving:
  - Available time for each stage < 450ps
- The 65nm CMOS process:
  - High speed and low parasitics
    - Fast switches
    - Good Ft
    - Good sampling linearity
  - But not fast enough
  - Poor gain and output impedance
  - Digital assistance is required

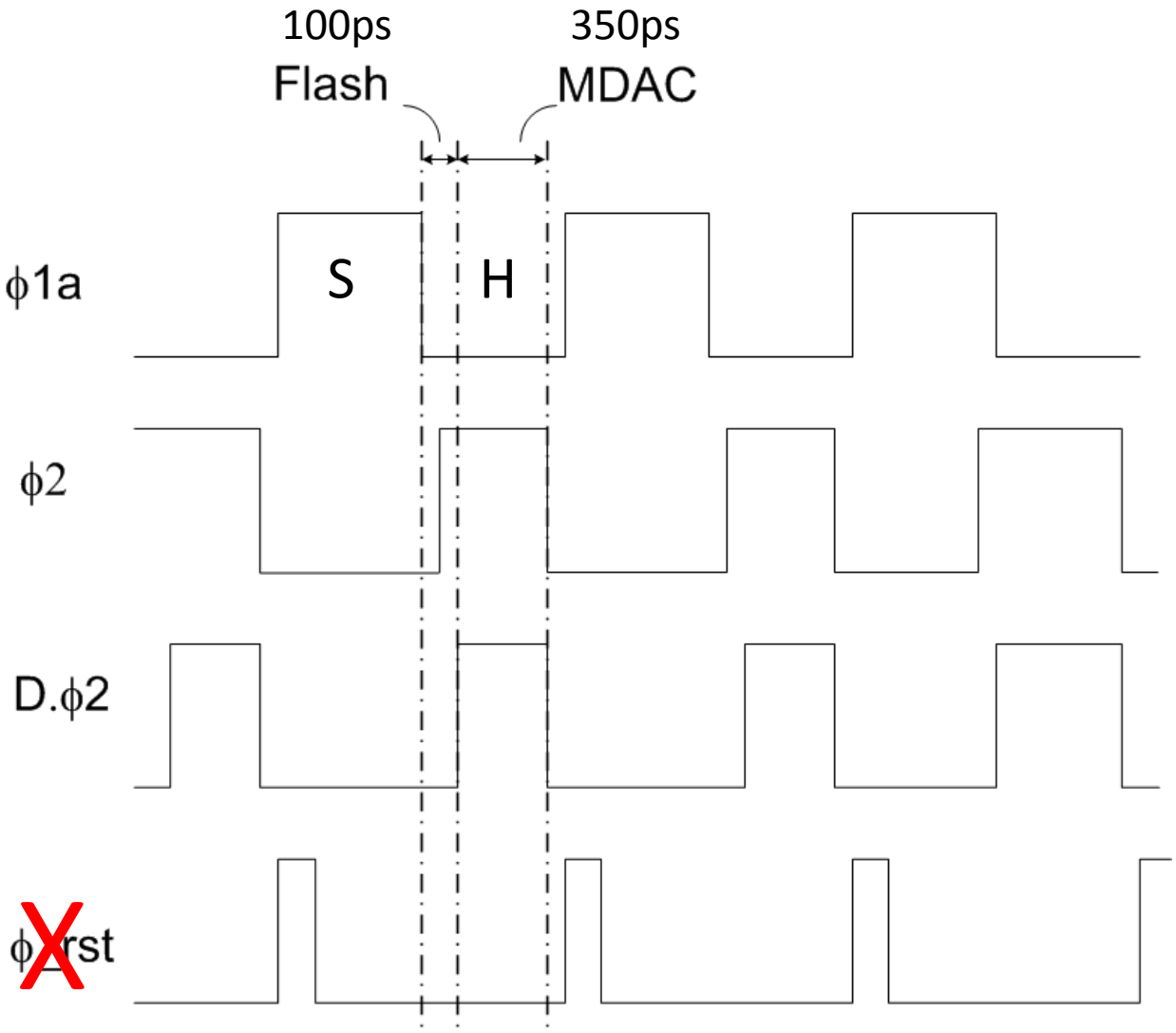
Pipeline Architecture



Stage-1 MDAC



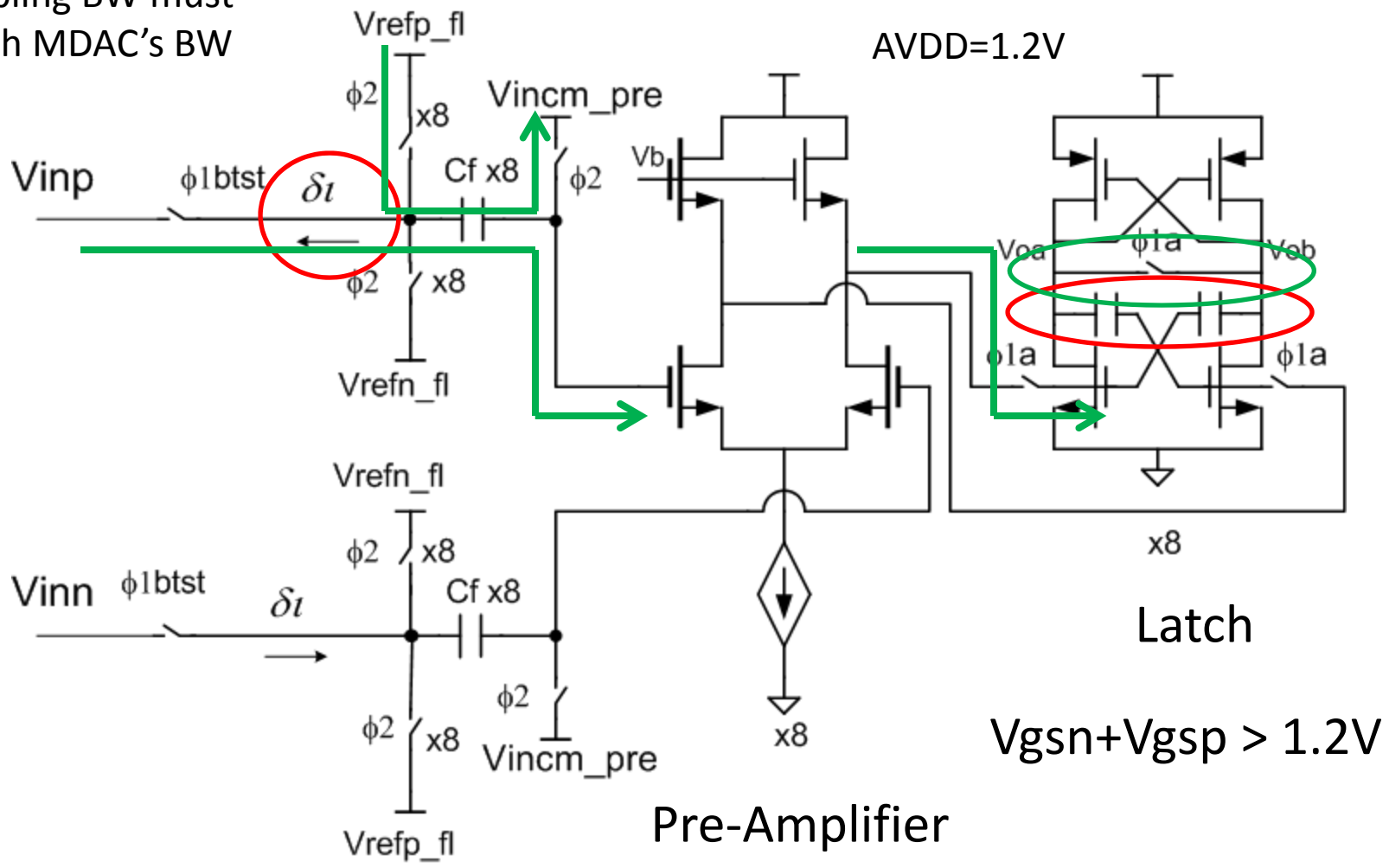
Stage-1 Timing



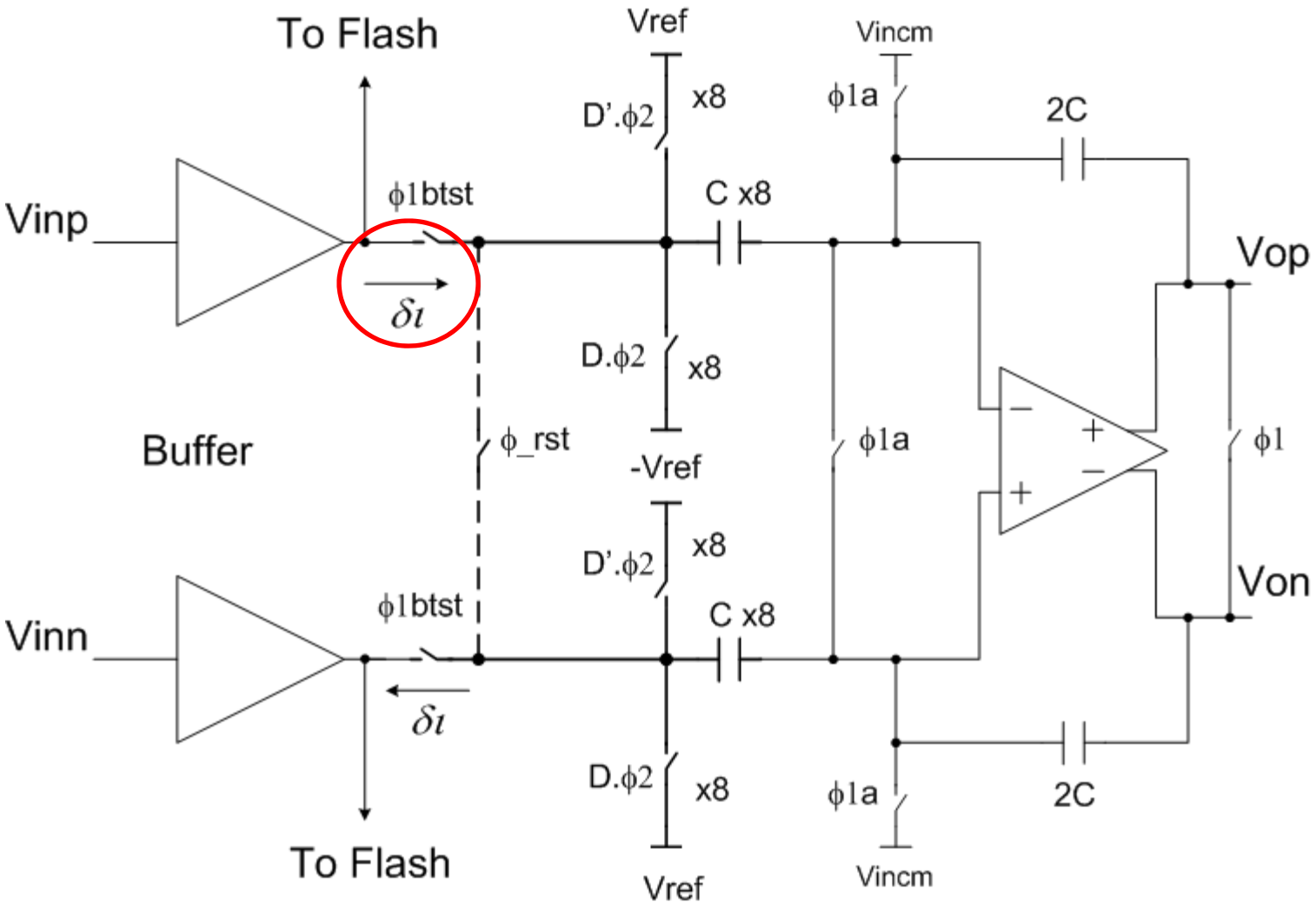
Kick-back Calibration instead of resetting

Stage-1 Flash

Sampling BW must match MDAC's BW

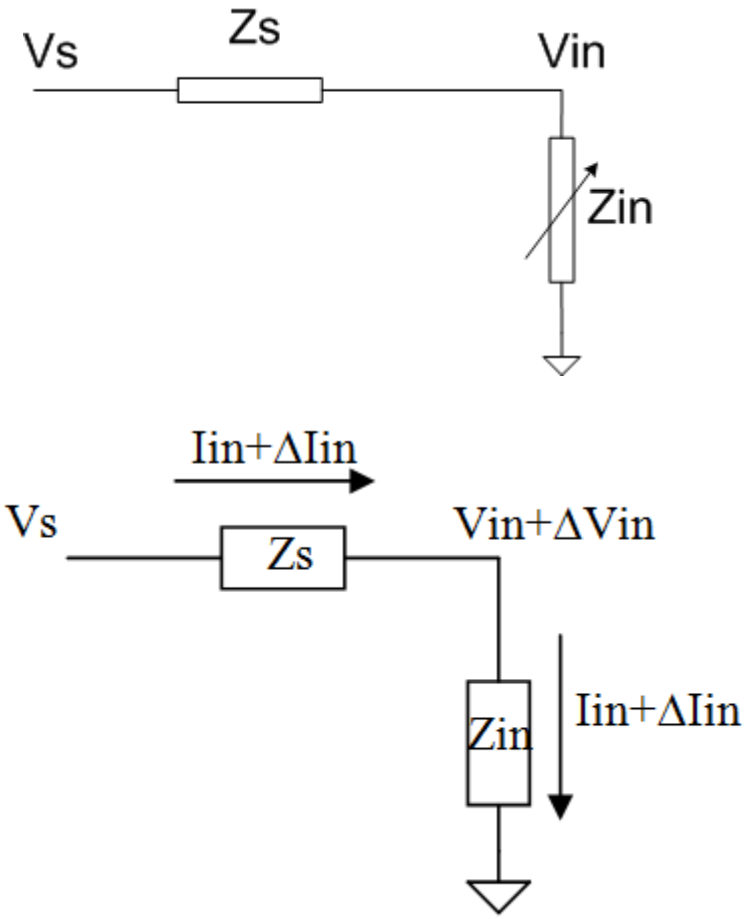


Stage-1 MDAC



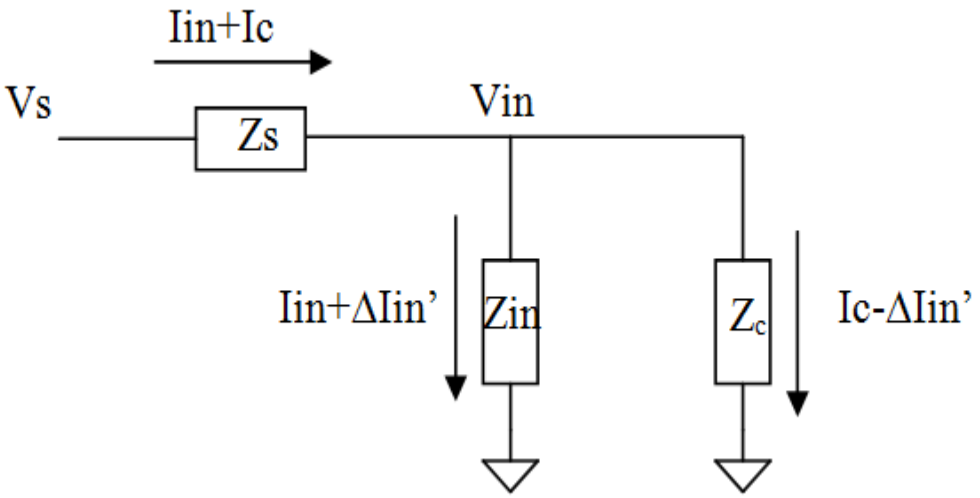
Tracking Non-linearity

- The non-linearity in Zin causes a non-linear current to flow in Zs
- The higher the non-linear current, the worse the distortion
- The higher Zs the worse the distortion



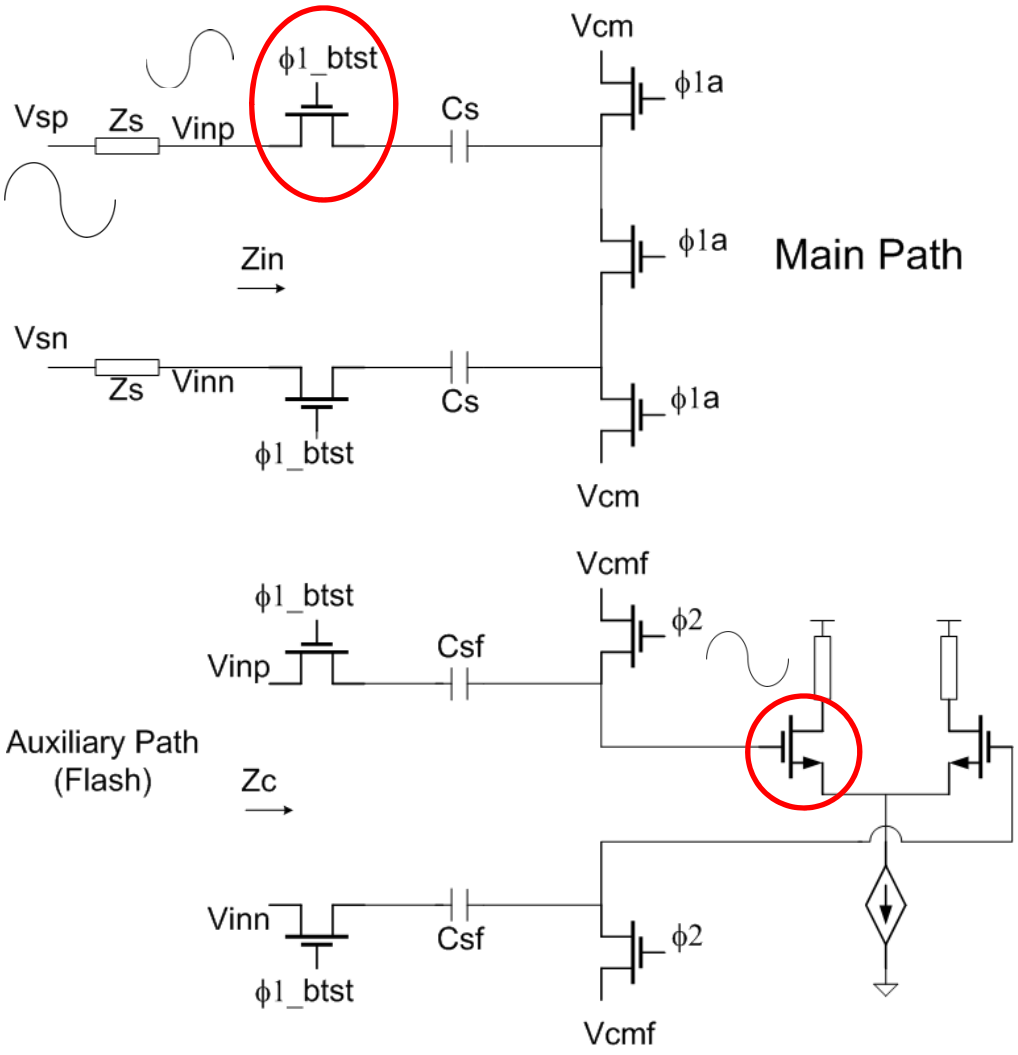
Distortion Cancellation

- An opposite non-linearity can be employed to cancel or reduce the non-linear current flowing in Zs
- It also reduces the non-linear current in the main branch



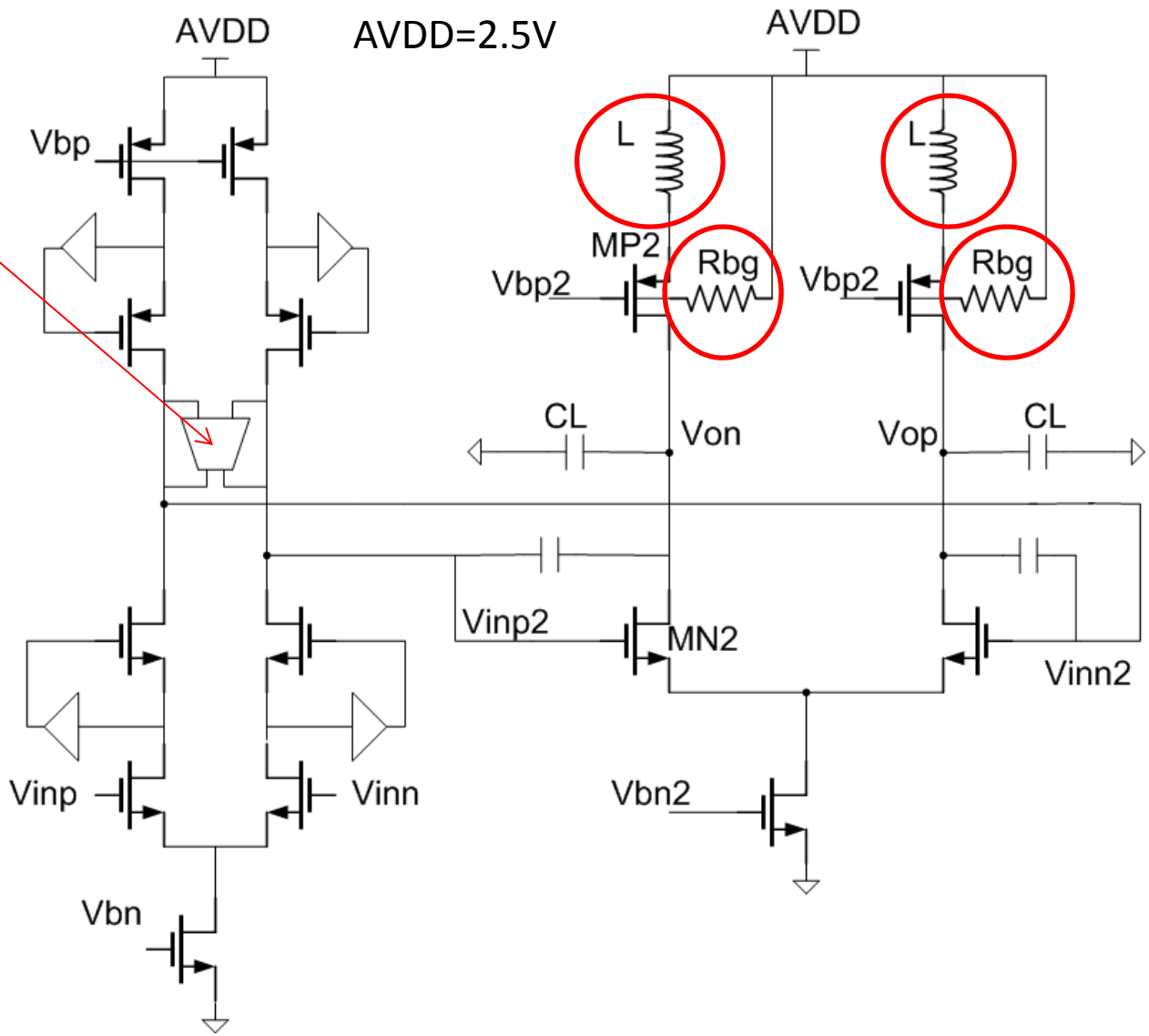
Examples of Distortion Cancellation Using the Stage-1 Flash

- Improves MDAC distortion by 3-6 dB
- Independent of process, temperature, and supply
- Improvement increases as driver impedance increases
- Actual total improvement of 6-12 dB



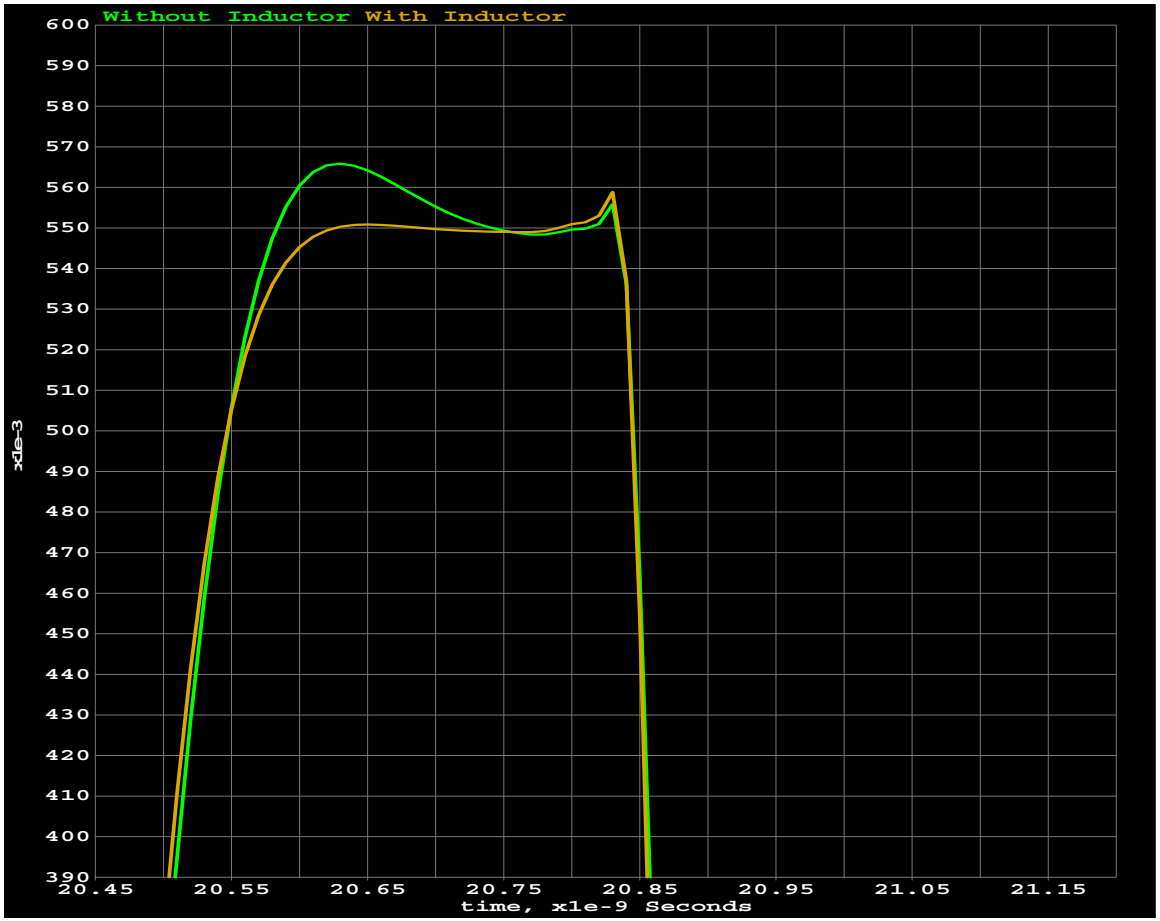
MDAC Amplifier

- Positive feedback circuit to enhance gain
- Floating back-gate to reduce parasitics
- Using inductors to improve settling time and reduce power consumption



Performance Comparison
Power saving of 40%

- Inductance value is given by L ~ C/gm
- Not very sensitive to variation in inductance value
- Employed in first 2 stages



Digital Calibration

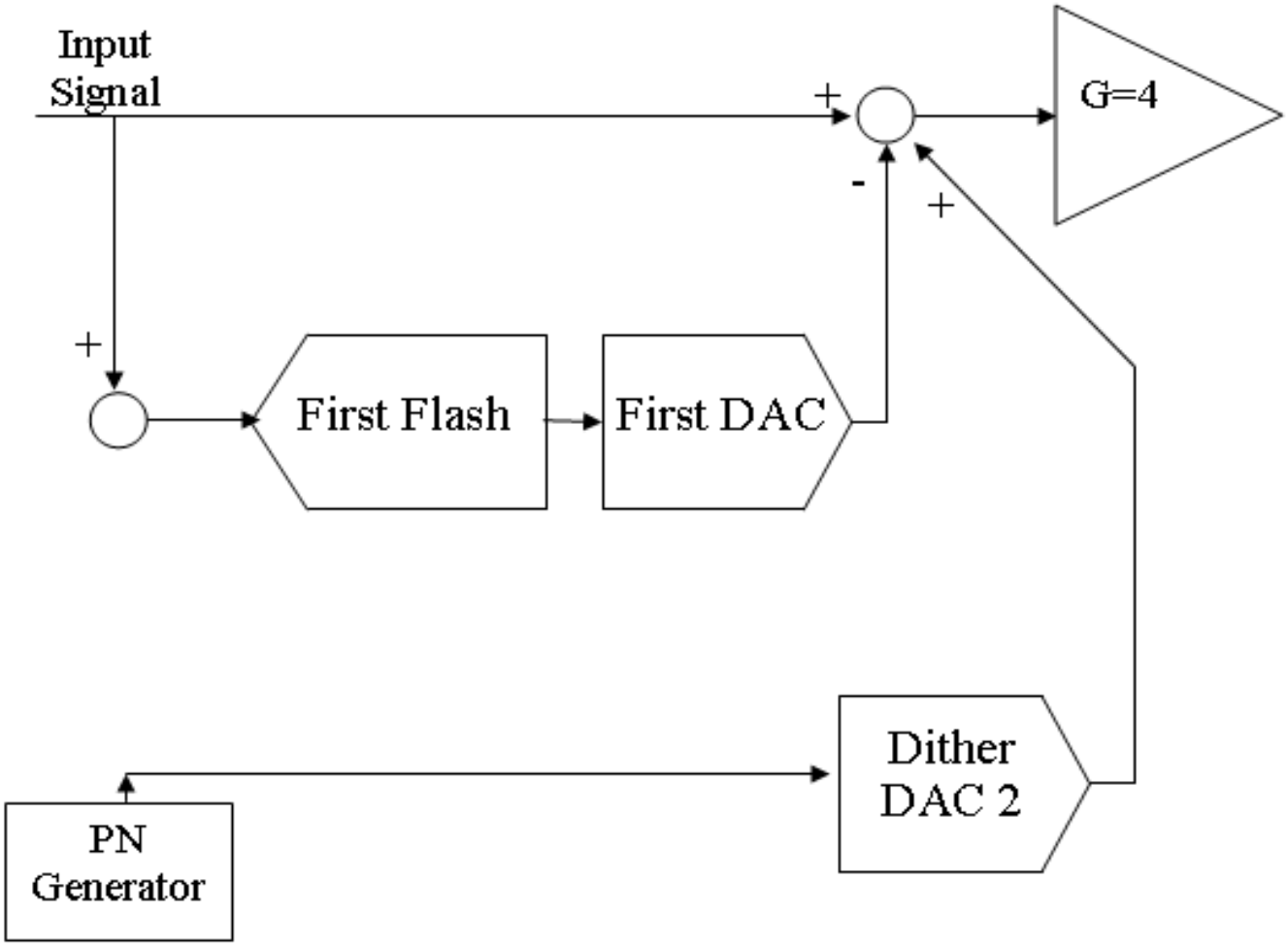
- Three kinds of calibration:
  - Inter-stage gain error calibration (IGE)
  - Inter-stage memory error calibration (IME)
  - Kick-back calibration (KB)

- Amplifier DC open loop gain is about 75-80dB
  - => IGE calibration is needed

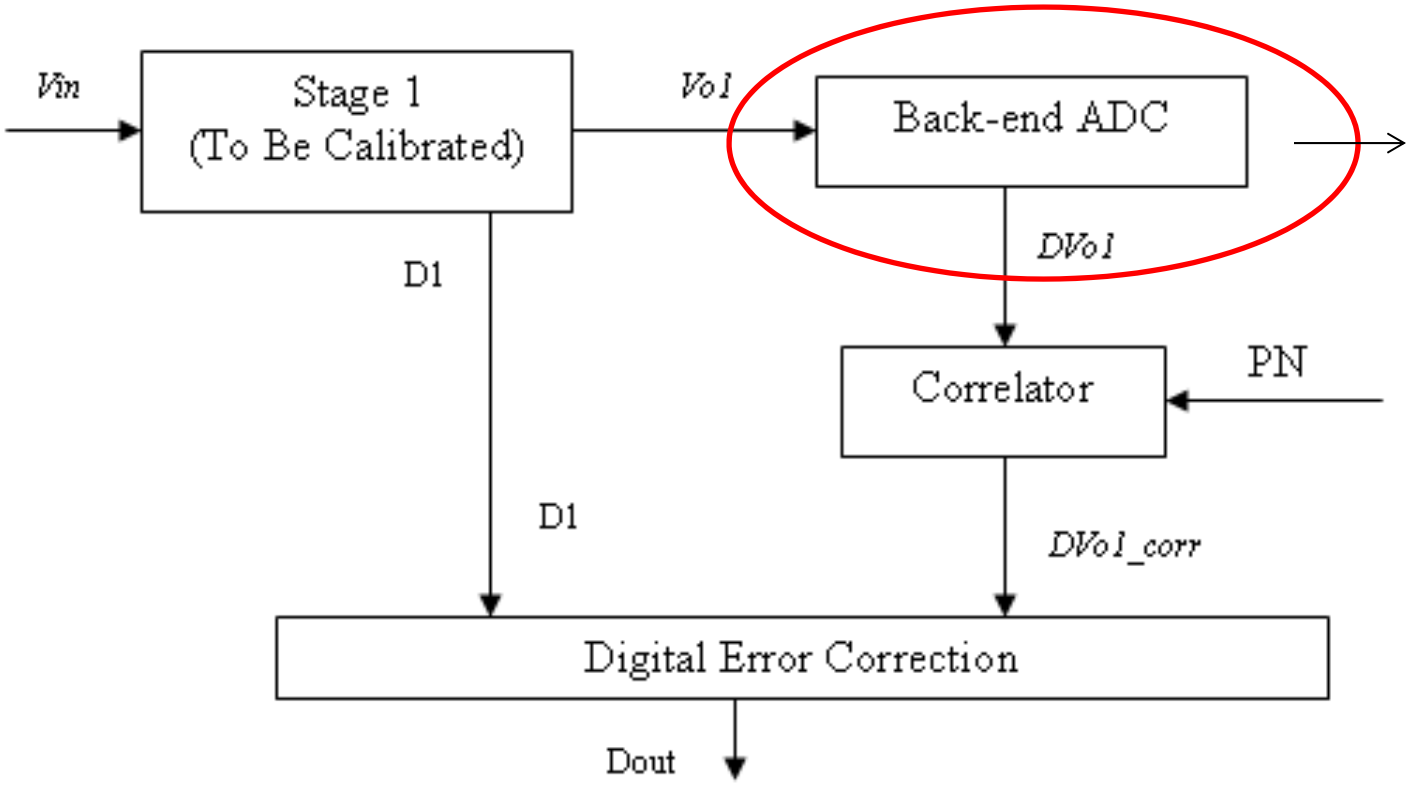
- IGE calibration also corrects for settling errors

- IME calibration corrects for errors due to capacitor dielectric relaxation/absorption and incomplete resetting

Correlation-Based Calibration
Random Signal is injected in the MDAC



Correlation-Based Calibration
Random Signal is injected in the MDAC

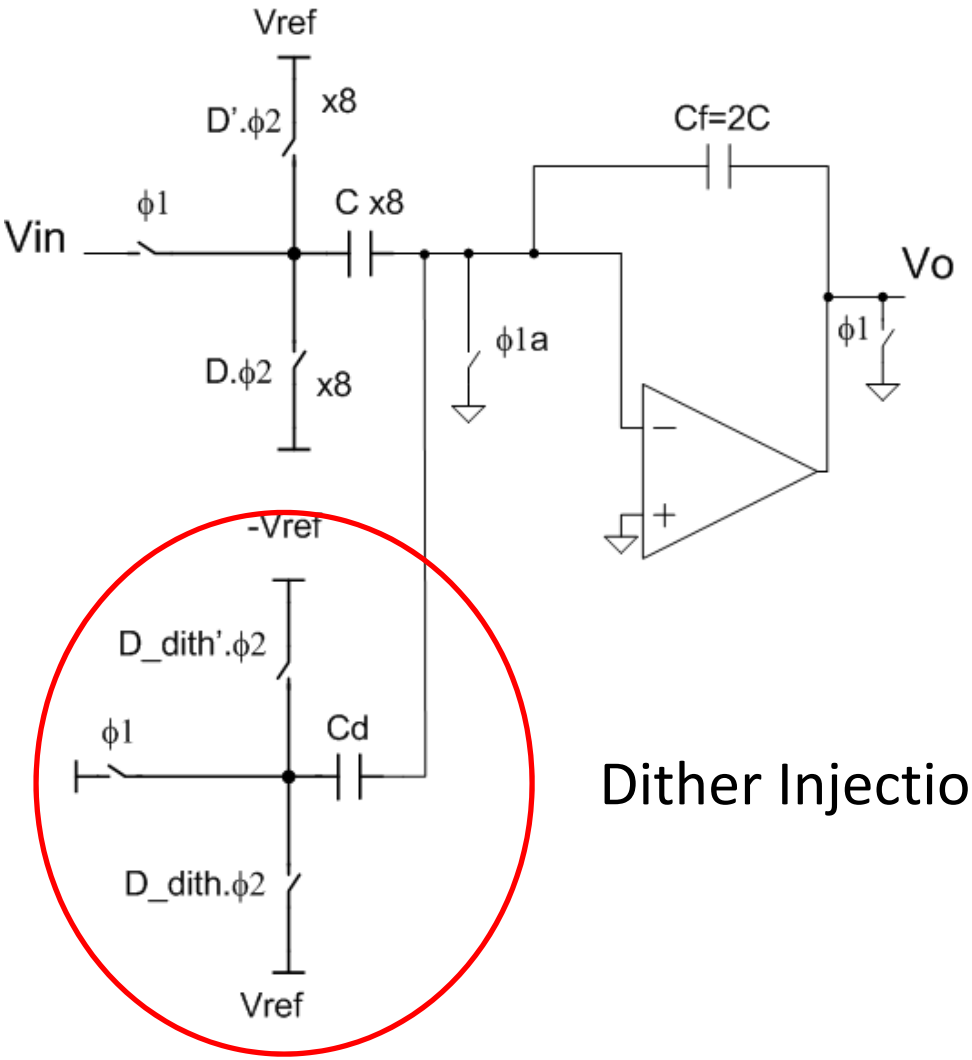


Must have adequate accuracy

LMS Algorithm $$Ge_{n+1} = Ge_n - \mu * Vd * [Vd * Ge_n - V_{01}]$$

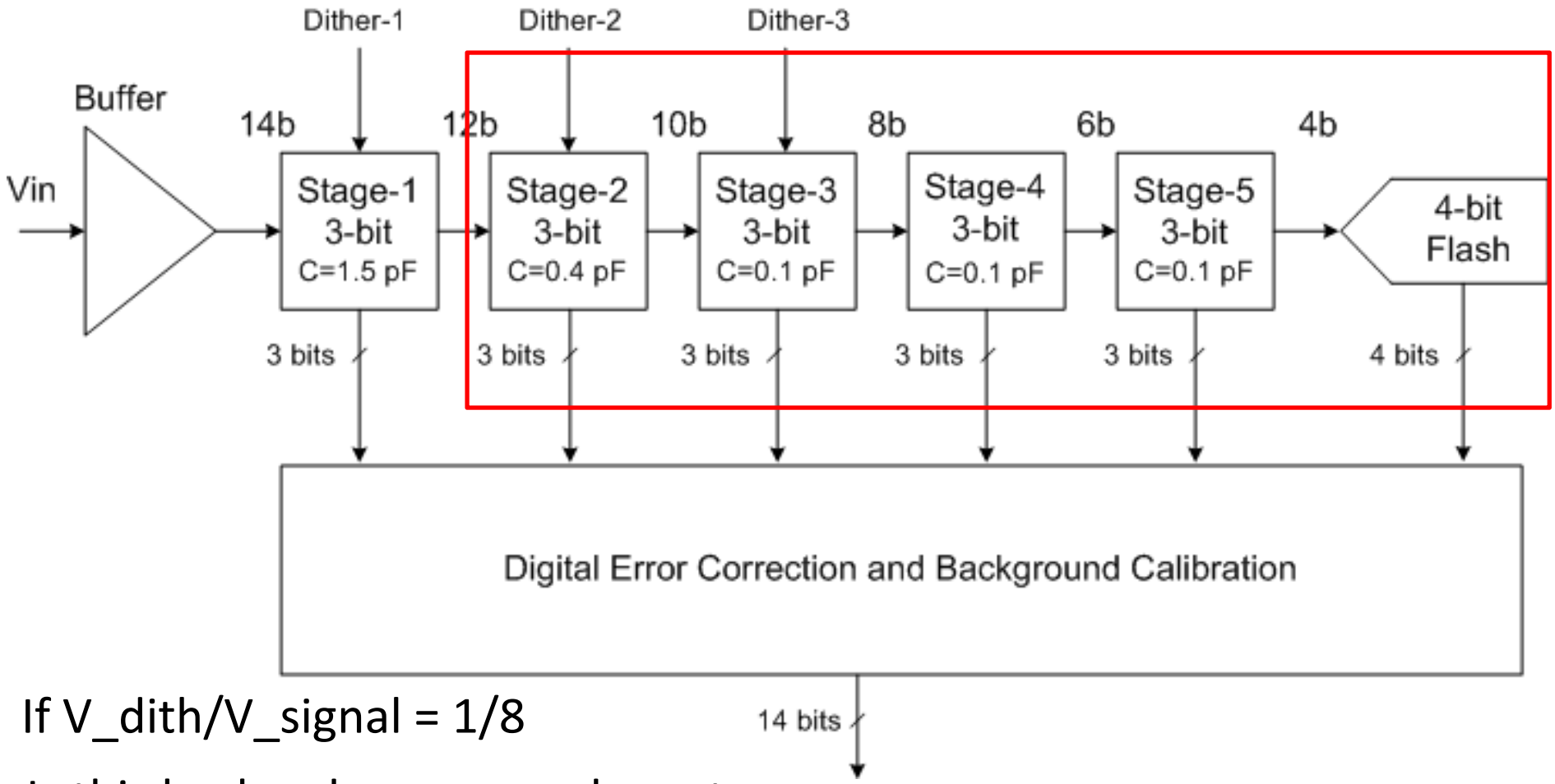
Correlation-Based Calibration
Random Signal is injected in the MDAC

- A portion of the correction range is consumed by the calibration random sequence
- This can cause a significant power overhead
- It is desirable to minimize the amplitude of the calibration signal (dither): V_dith



Dither Injection

But …



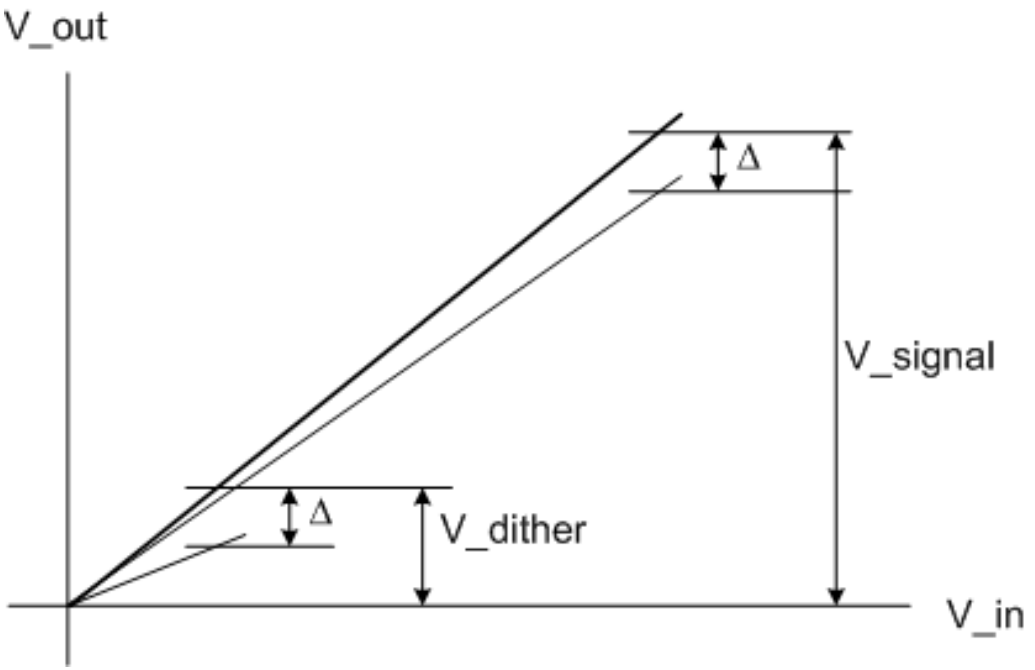
If V_dith/V_signal = 1/8

Is this backend accuracy adequate for the calibration signal?

No

Effect of Using a Small Dither

- The calibration accuracy is degraded by the ratio of:
  - V_dither/V_signal
- Degrades accuracy when using small dither for calibration
- We need to improve the linearity of the back-end by at least that ratio



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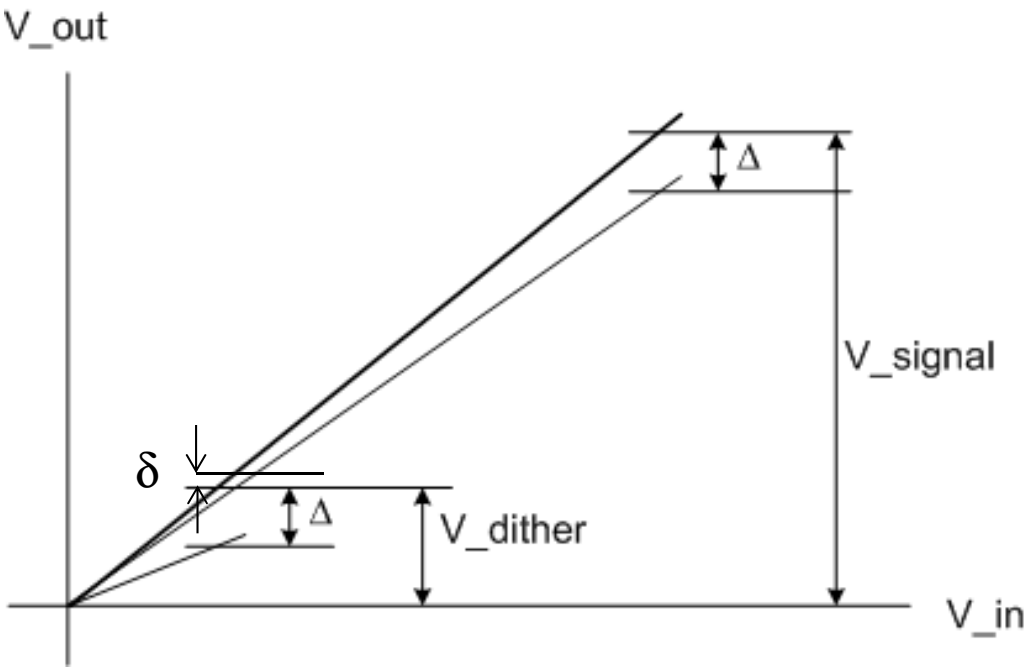

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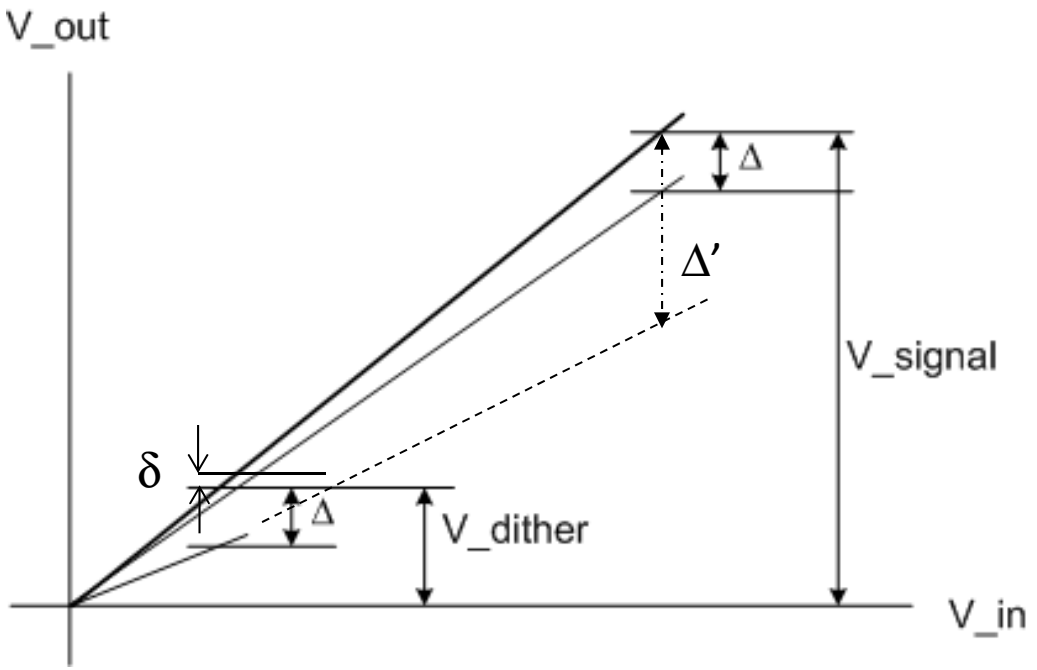
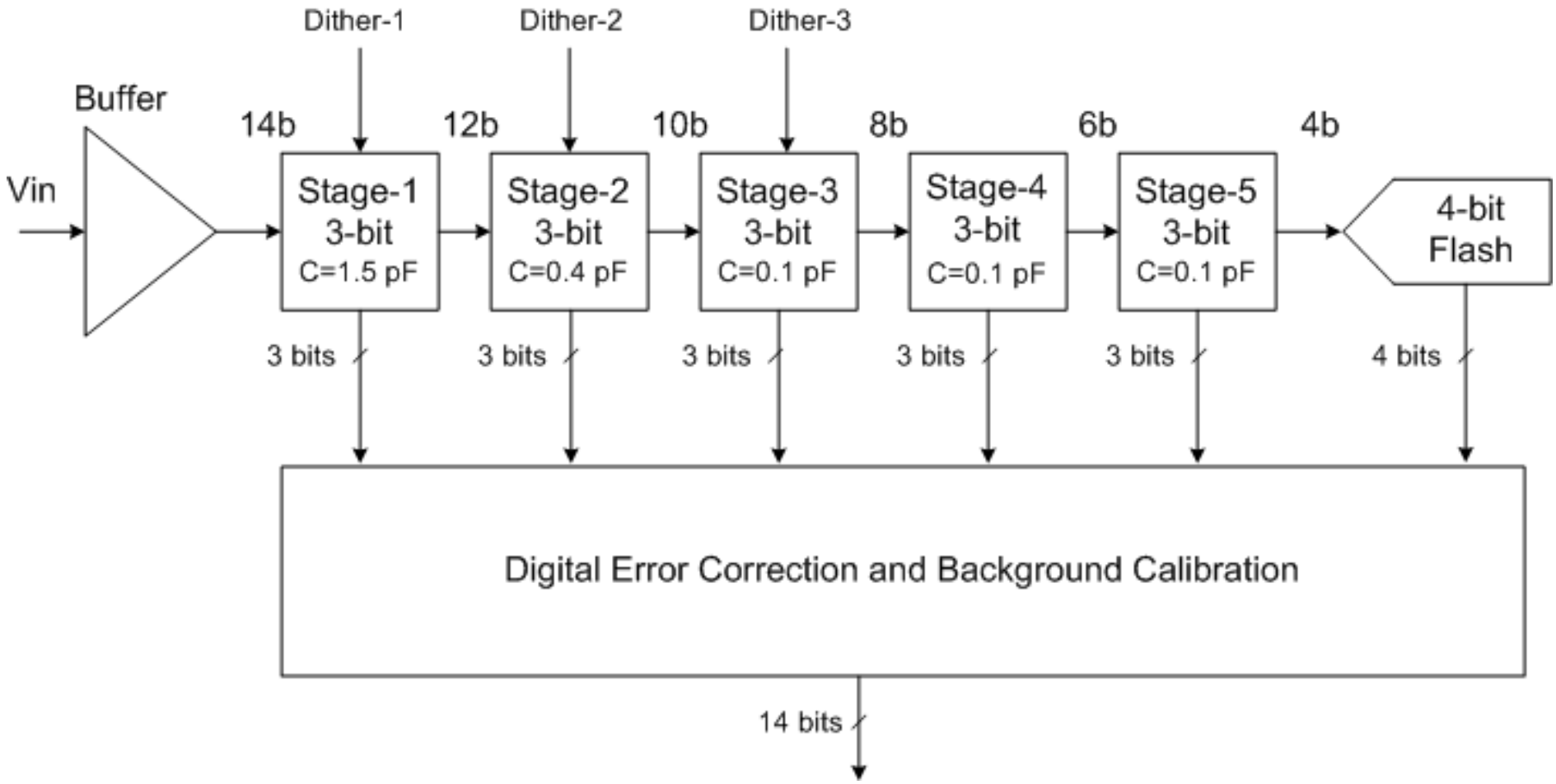
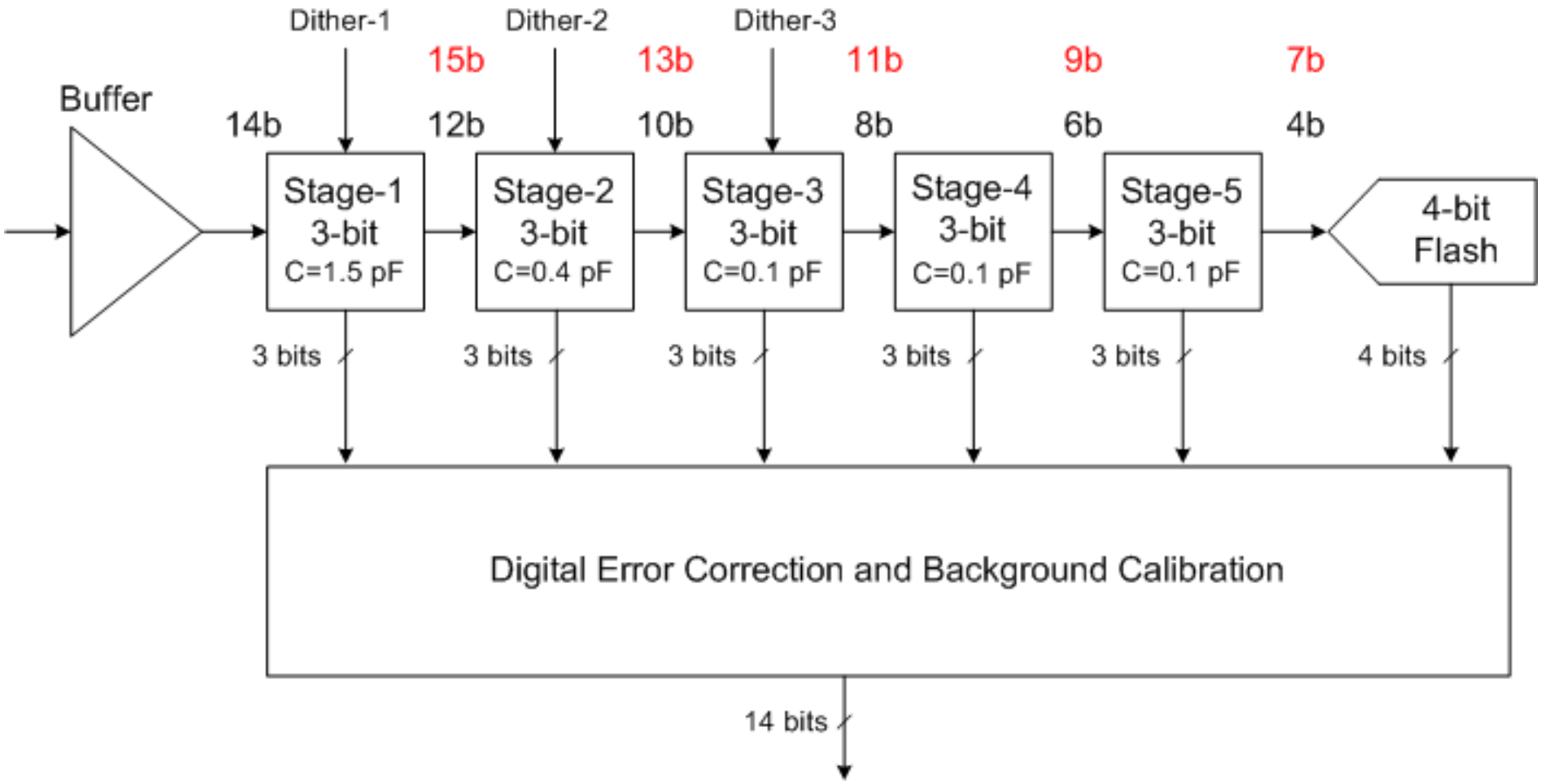


$\delta/\Delta = \Delta/\Delta' = V\_dither/V\_signal$

Accuracy of Pipeline Stages

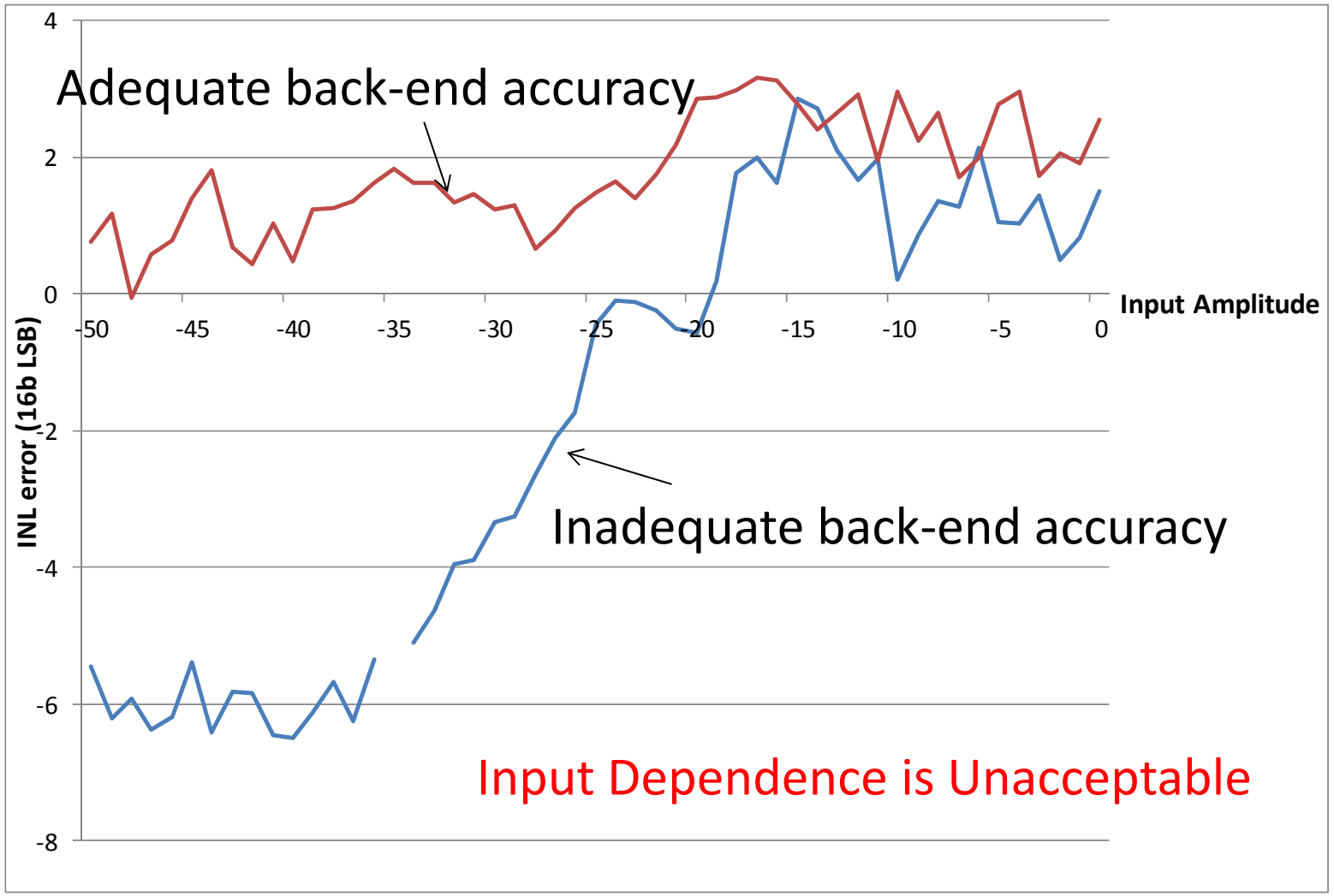


Accuracy of Pipeline Stages



For V_dither/V_signal = 1/8

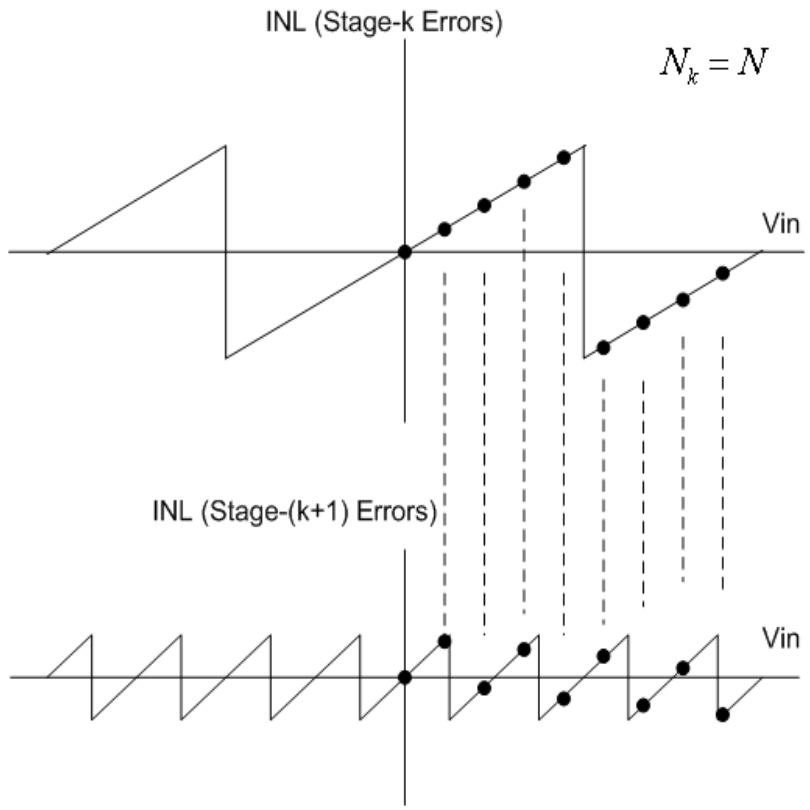
Example of the Problem
INL vs Input Amplitude (Frozen Cal)



Proposed Solution

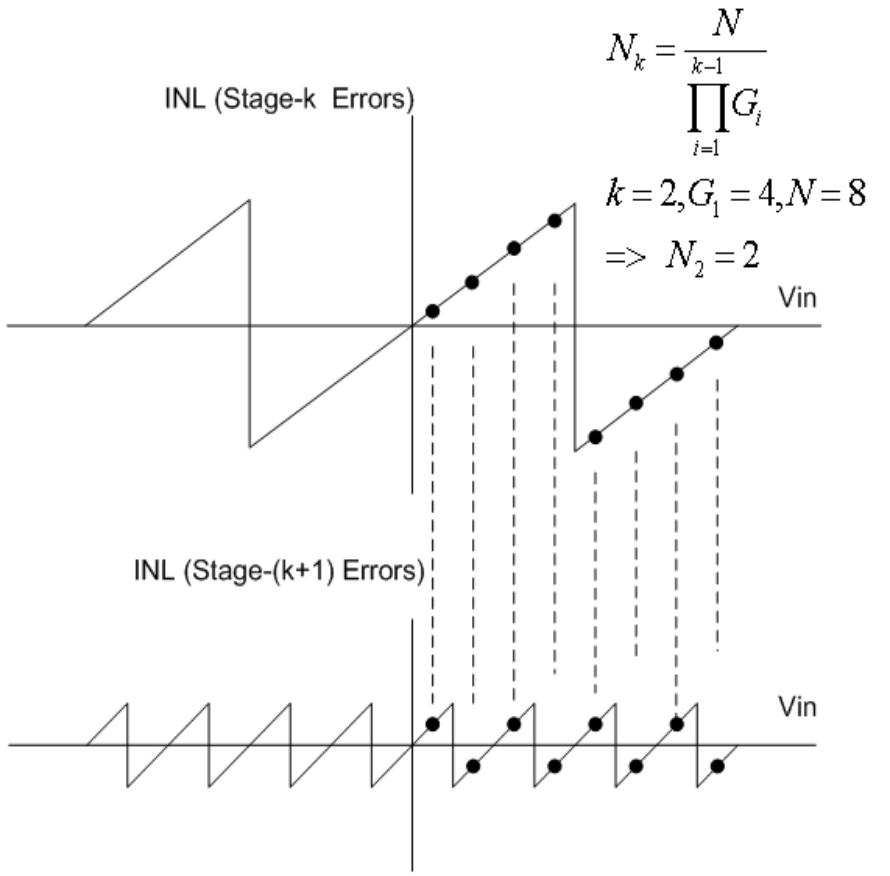
- Inject a small dither signal in the MDAC
- Since the dither is small, we only use a small part of the correction range => small power overhead
- Use multi-level dither (odd number) in every stage to improve accuracy of the back-end (9 levels => 3.2-bits)
- Dynamic element matching is utilized
- Ensure effective dither propagation down the pipeline such that the number of dither levels for each stage is adequate for the required accuracy

Dither Propagation



Dither using odd number of levels (9)

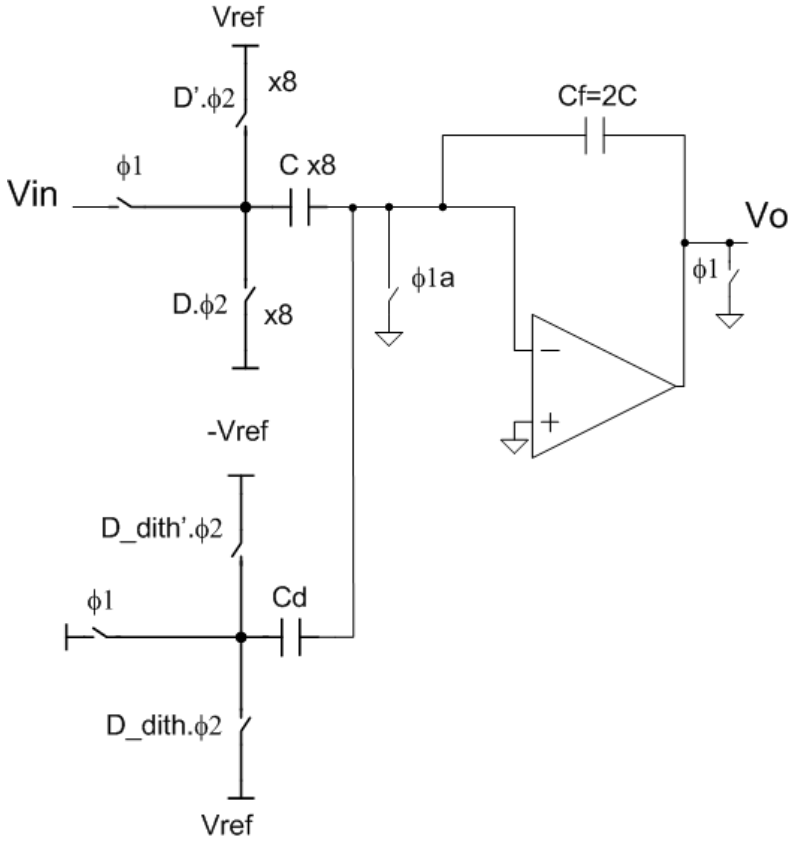
✓



Dither using even number of levels (8)

X

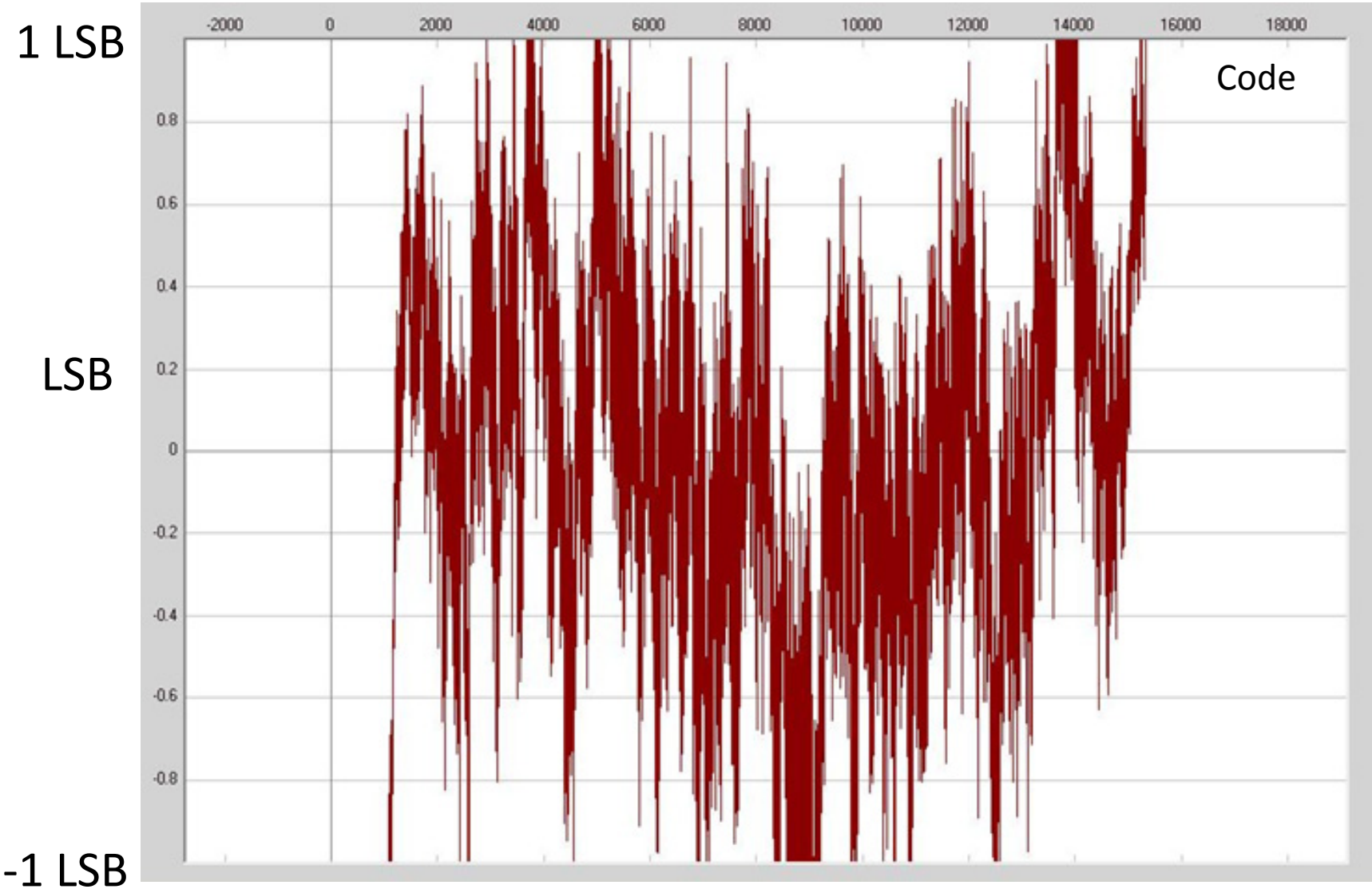
The IME/IGE Calibration Correlator



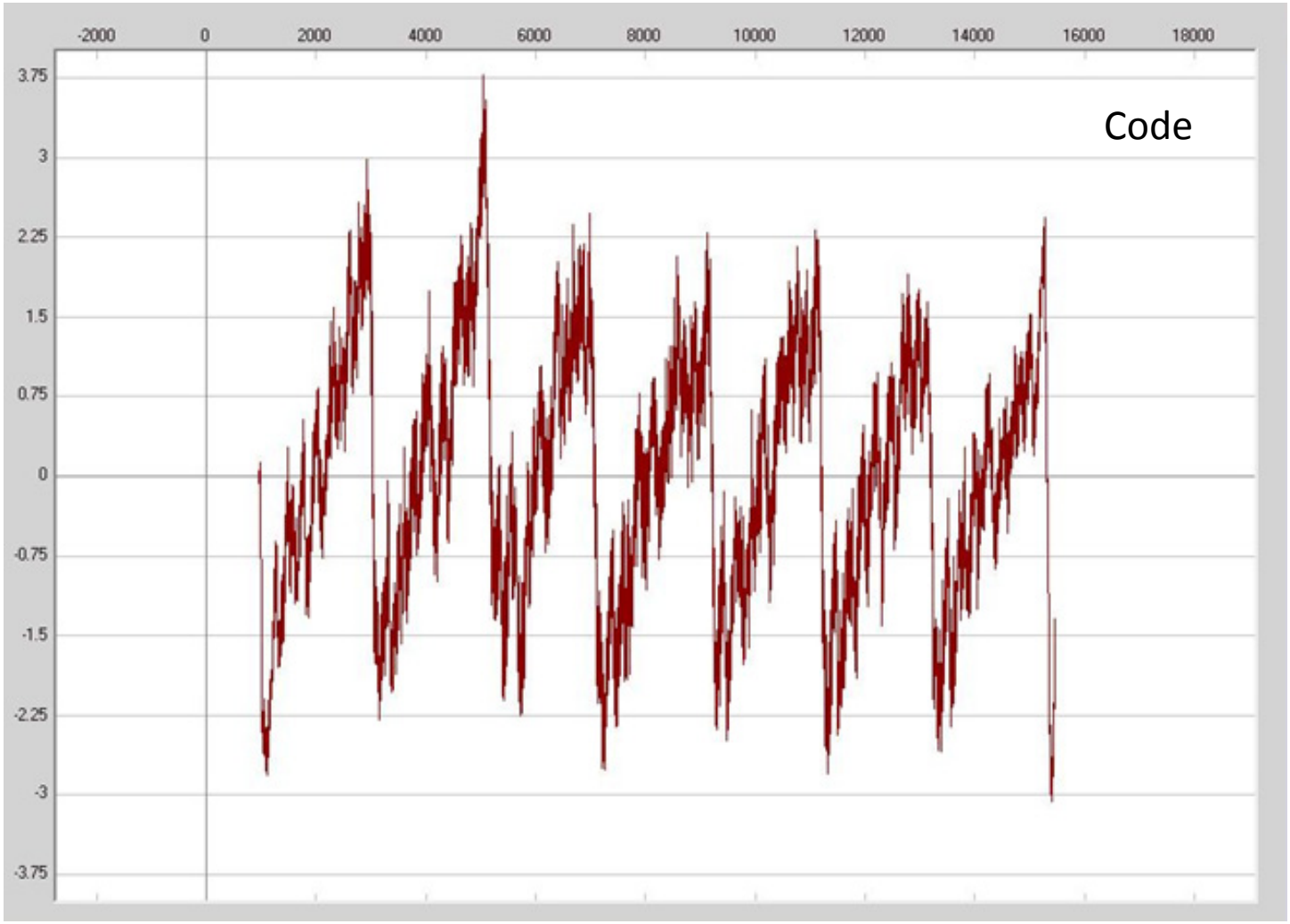
$$Ge_{n+1,k} = Ge_{n,k} - \mu * Vd[n-k] * (Vd[n-k] * Ge_{n,k} - V_R[n])$$

$$V_{R\_cal}[n] = \sum_{k=0}^{M} V_R[n-k] \times Ge_{n,k}$$

INL at Room Temperature



INL at High Temperature
Calibration OFF

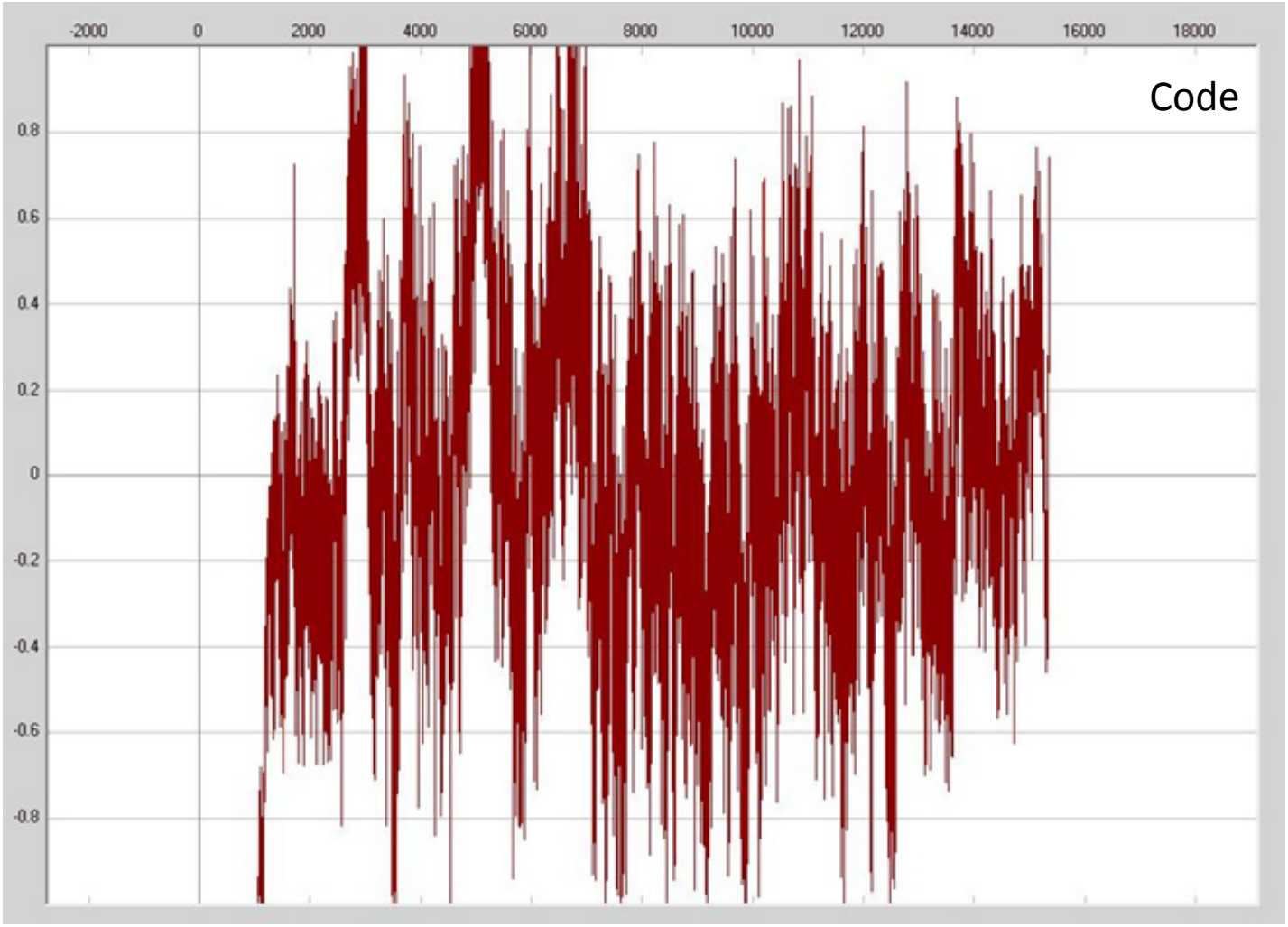


INL at High Temperature
Calibration ON

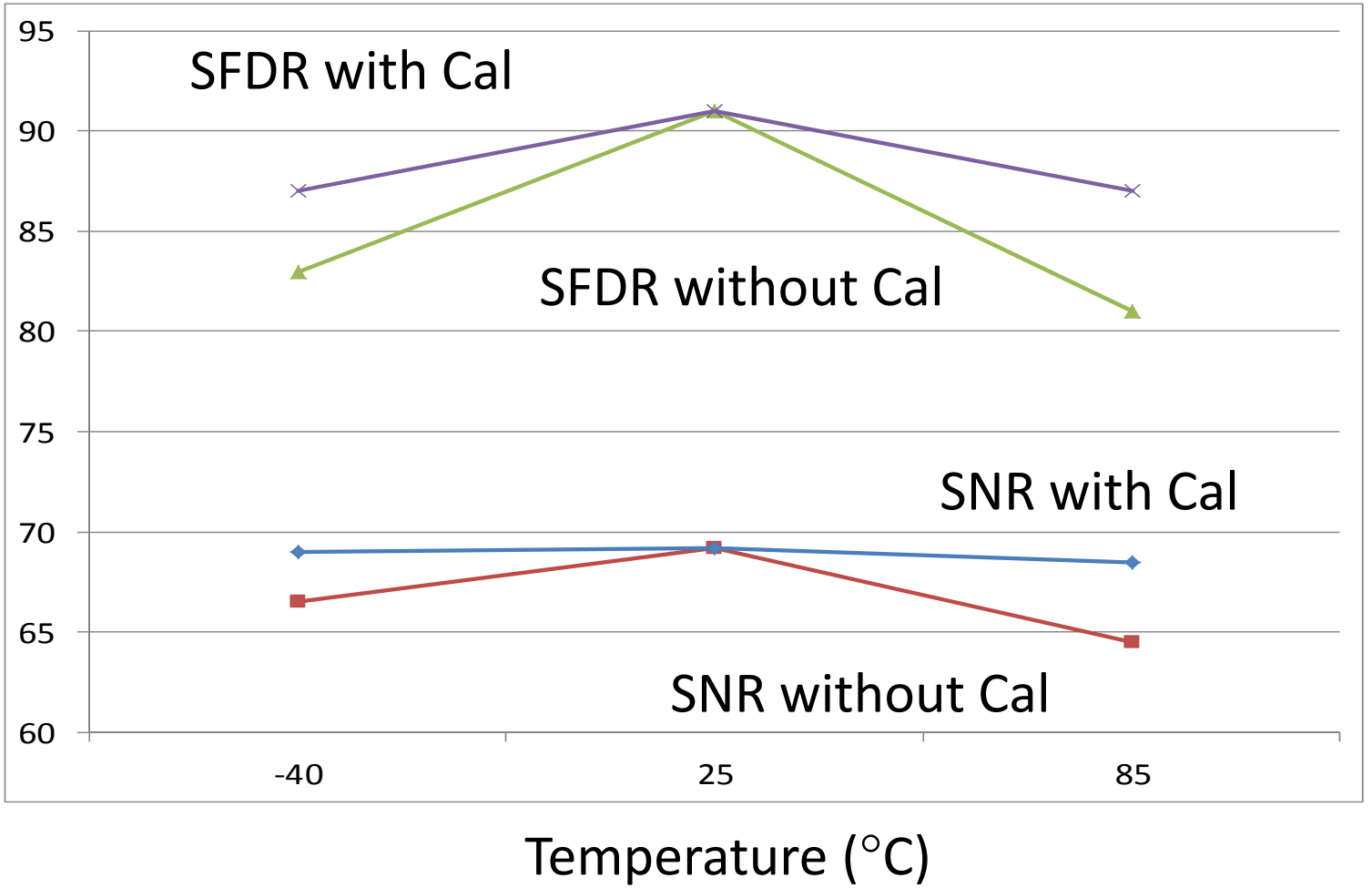
1 LSB

LSB

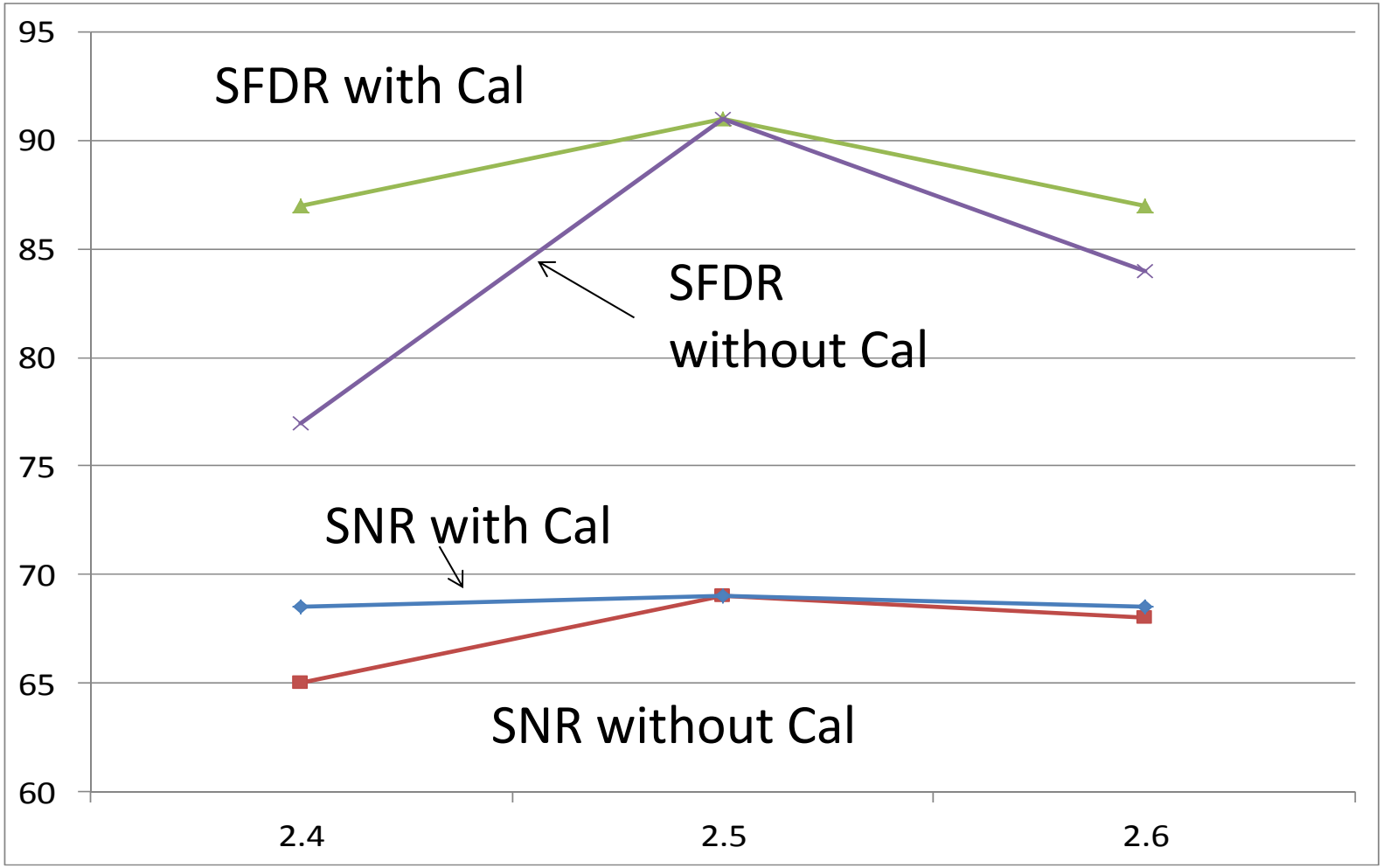
-1 LSB



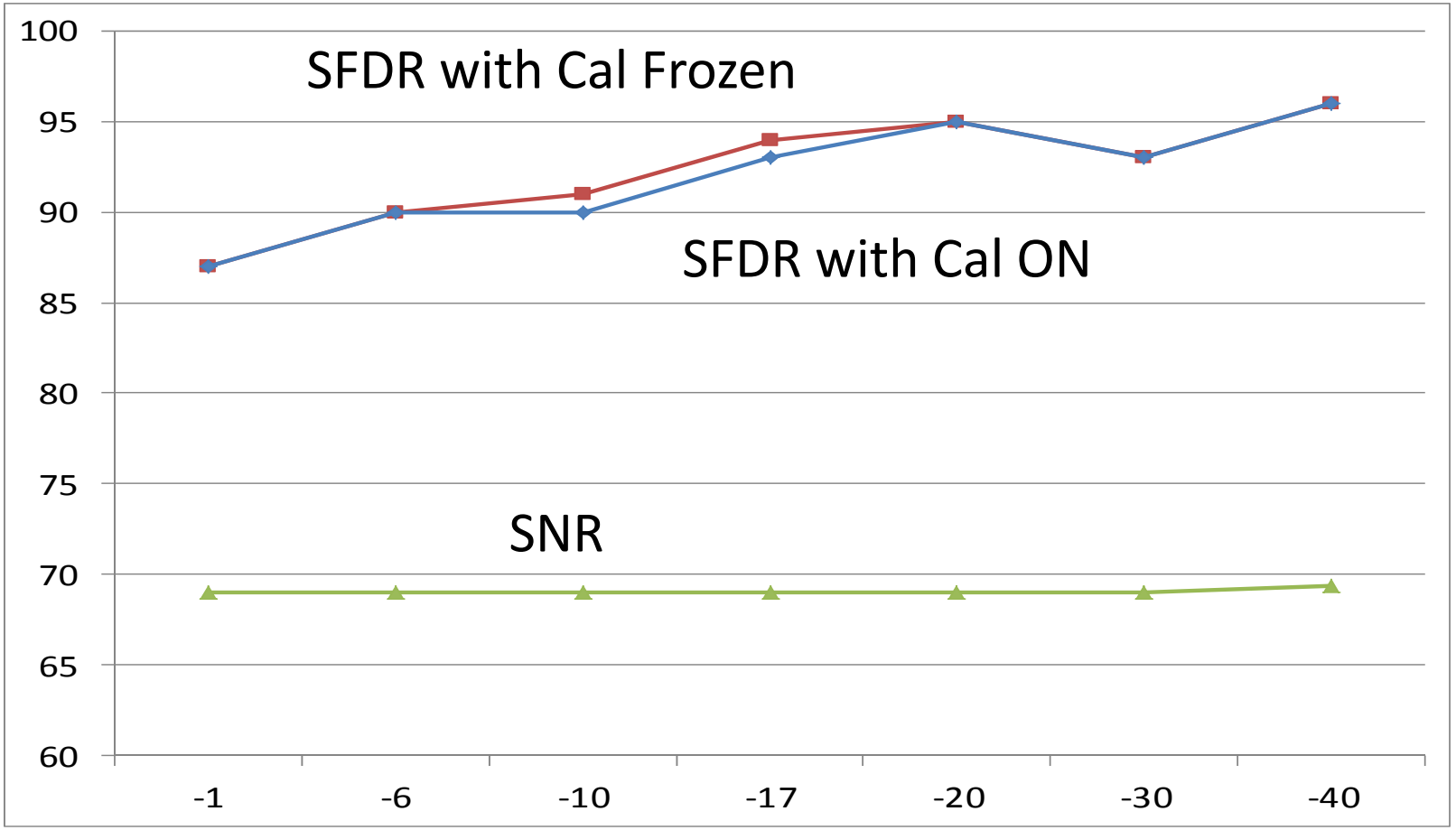
IGE Calibration Temperature Testing
SNR and SFDR



IGE Calibration Supply Testing
SNR and SFDR

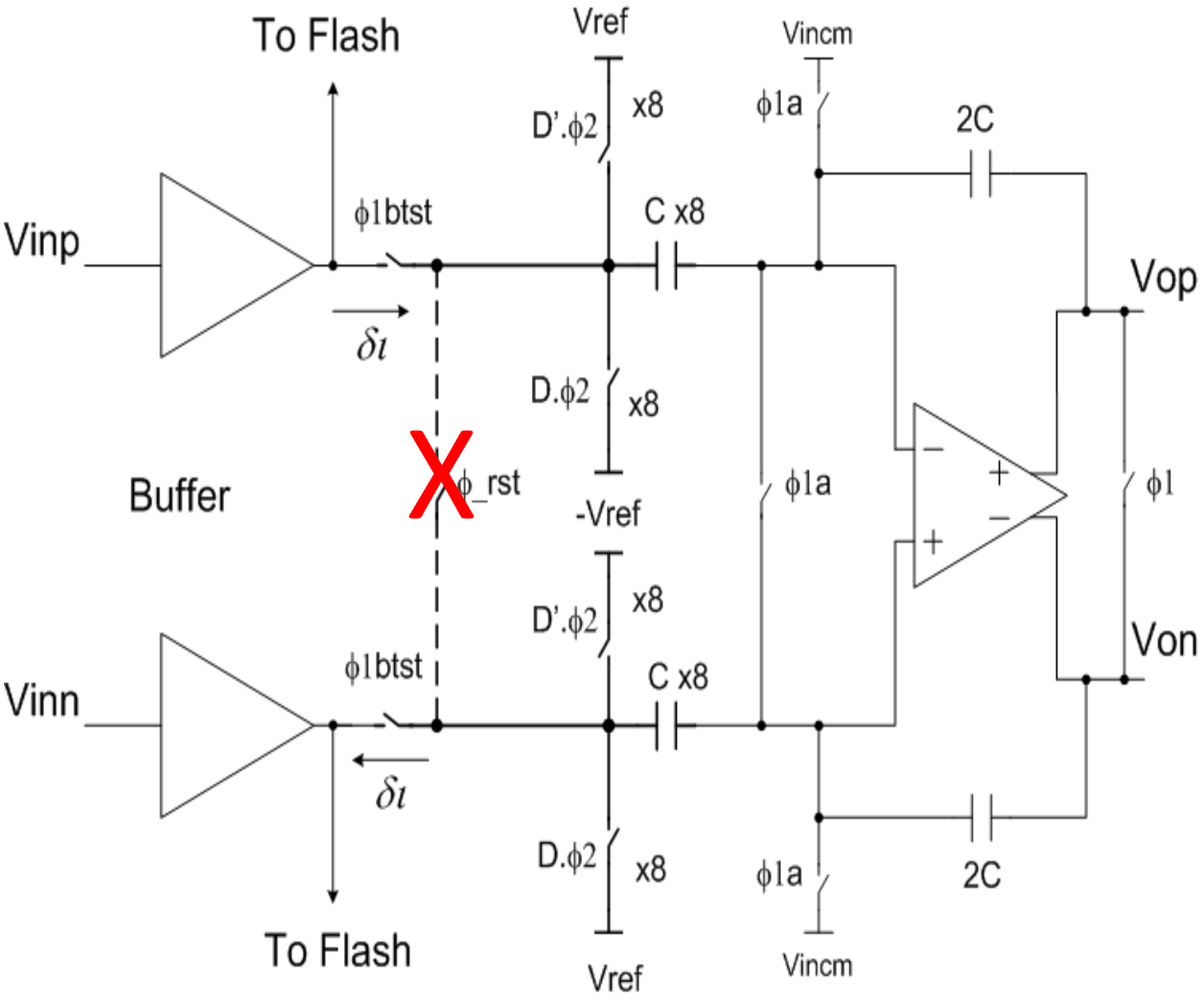


Performance vs Input Amplitude With IGE Cal ON and Frozen



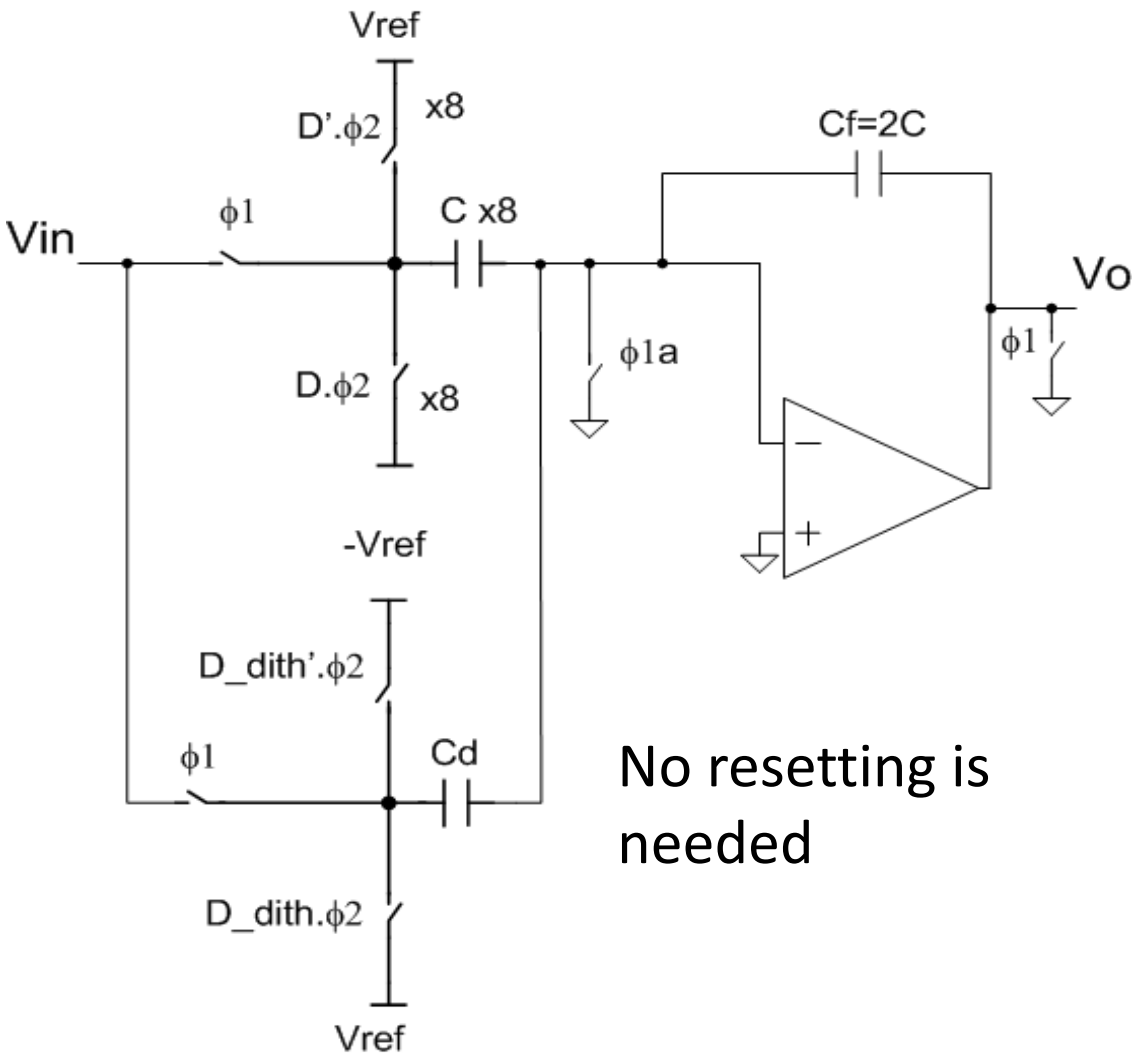
Front-end (Kick-back)

- Input sampling caps are used for the DAC
- The caps are briefly reset before sampling to remove the non-linear charge
- Alternatively, KB calibration can be used



Kick-back Background Calibration

- The kick-back dither caps are connected to the input during the sample phase
- The dither kicks the input similar to the sampling capacitances' kick
- The dither's kick is sampled on the total capacitances and propagates down the pipeline



No resetting is needed

Kick-back Background Calibration

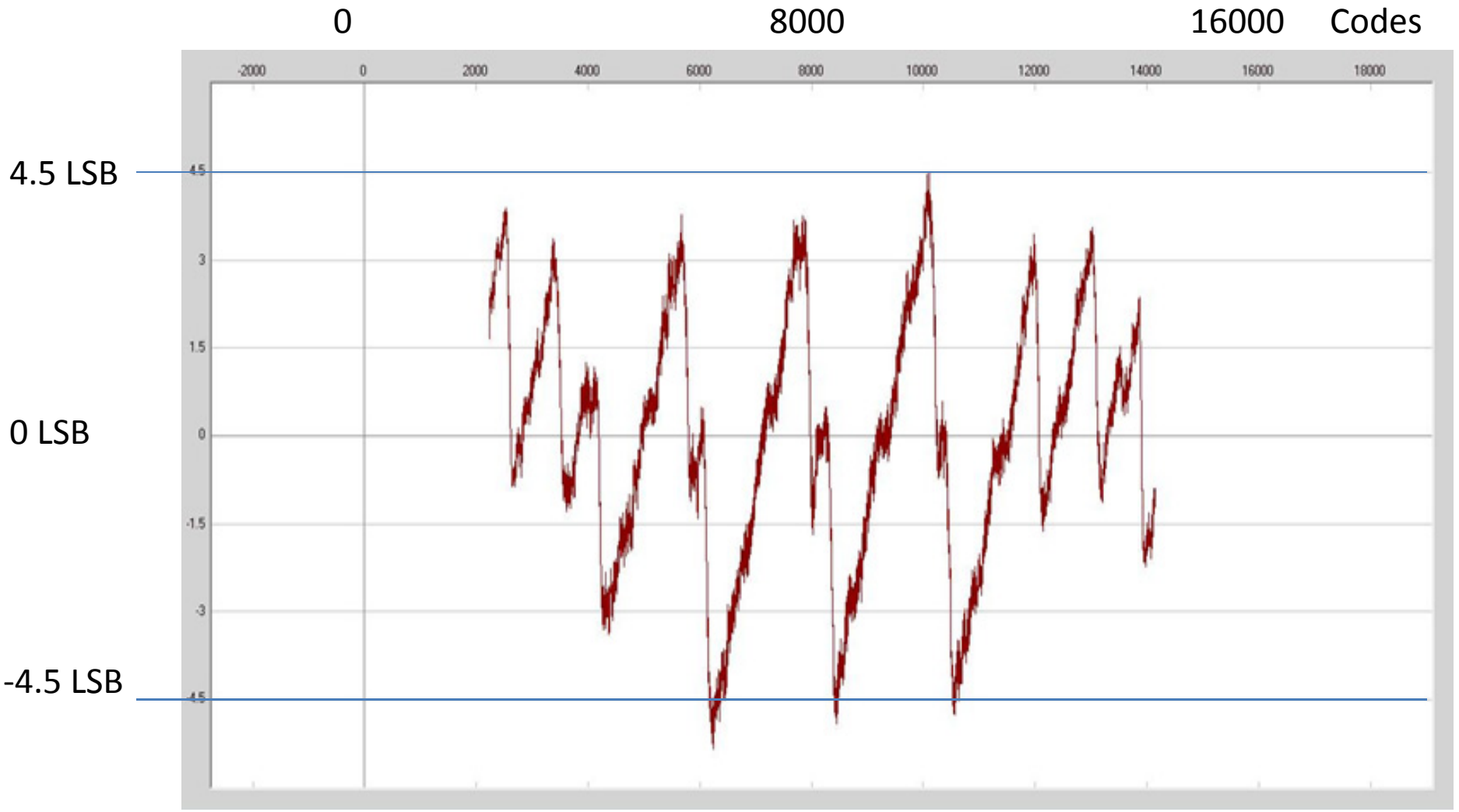
- The LMS algorithms is used to estimate the gain/correction coefficient *Gkb* of the dither's kick of the previous sample(s)

$$Gkb_{n+1,k} = Gkb_{n,k} - \mu * Vd[n-k] * (Vd[n-k] * Gkb_{n,k} - V_{in}[n])$$

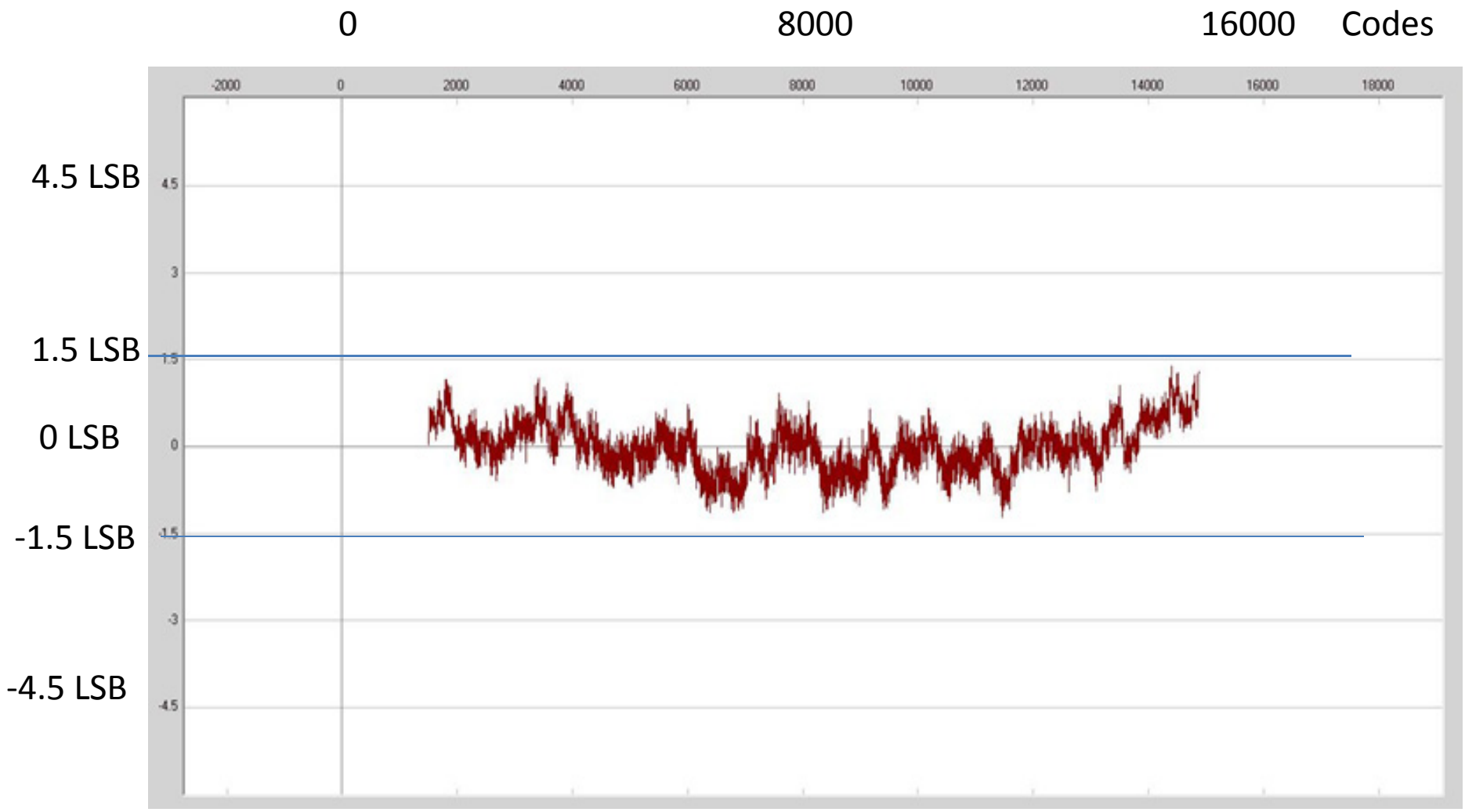
- The correction coefficient *Gkb* is applied to the previous stage-1 flash bits

$$V_{out\_kbcal}[n] = V_o[n] + \sum_{i=1}^{M_{kb}} D_1[n-i] \times G_{KB,i}$$

INL without Kick-back Calibration



INL with Kick-back Calibration



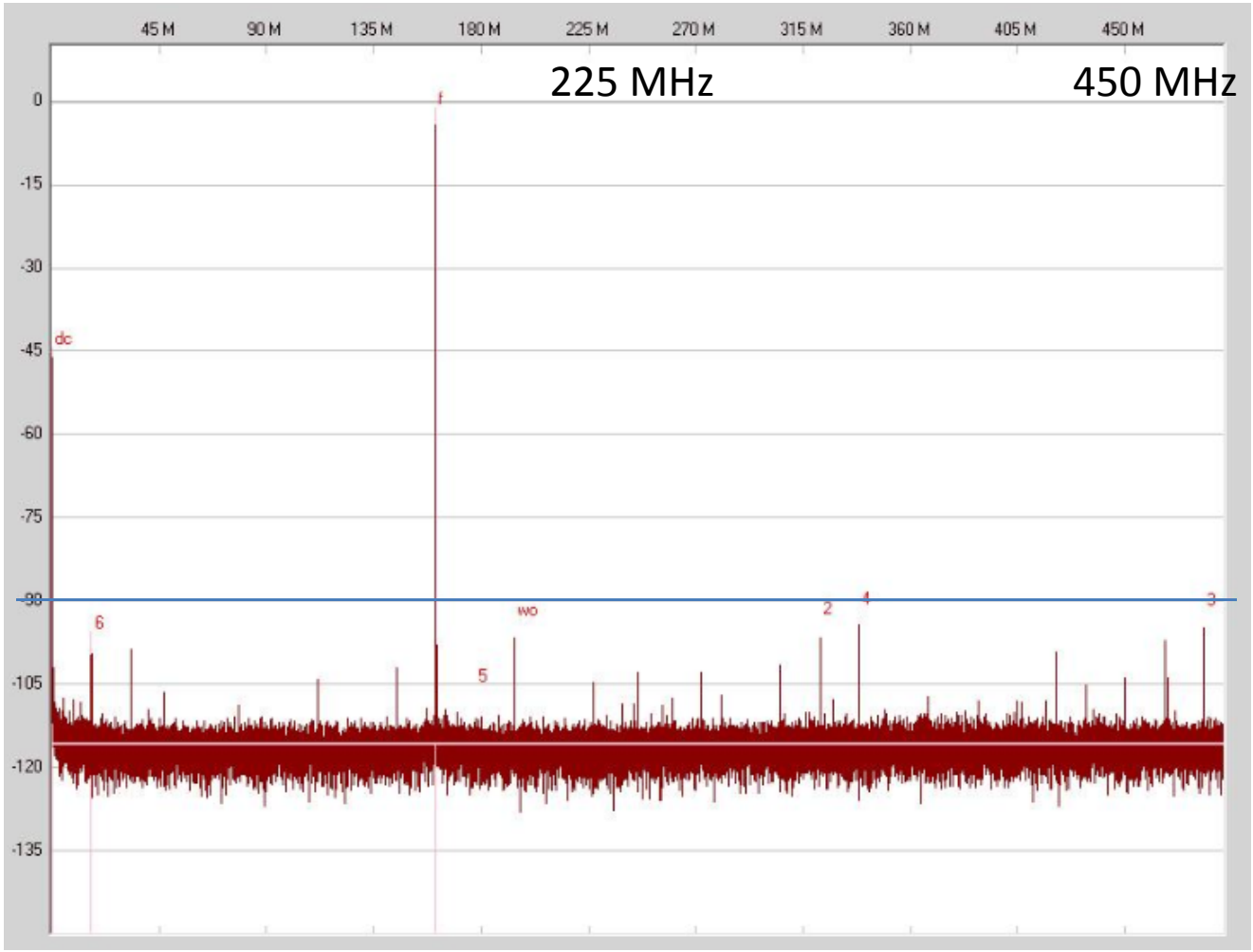
Performance Summary

	Without Calibration	With Calibration
SNDR (Fin=140MHz)	<62 dB	69 dB
SFDR (Fin=140MHz)	<70 dB	86 dB
INL	+/-15 LSB	+/-1 LSB
DNL	-1 LSB	+/-0.3 LSB
Noise Spectral Density (NSD)	-149 dB/Hz	-156 dB/Hz
Power	1.2 W	
Sample Rate	1 GS/s	
FOM=SNDR+10log(BW/Power)	155.2 dB	
Input Span	1.2Vpp to 2Vpp	
Jitter	50 fs	
Dimensions	6mm x 3mm	
Process	65nm CMOS	
Package for 2 ADCs	64-pin LFCSP (QFN)	

FFT at 1GS/s and Fin=160MHz
SFDR = 91dB at -1dBFS

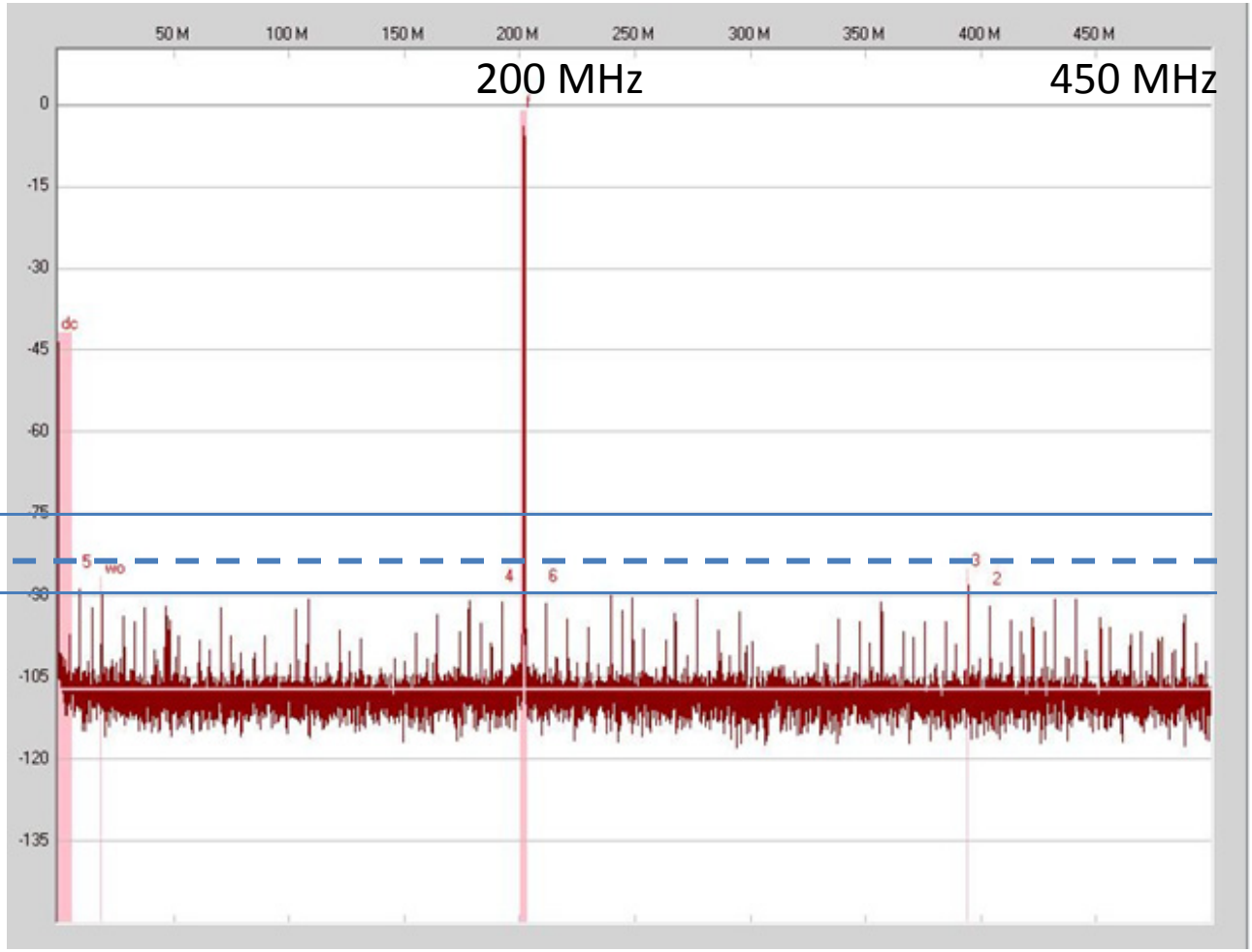
0 dB

-90 dB

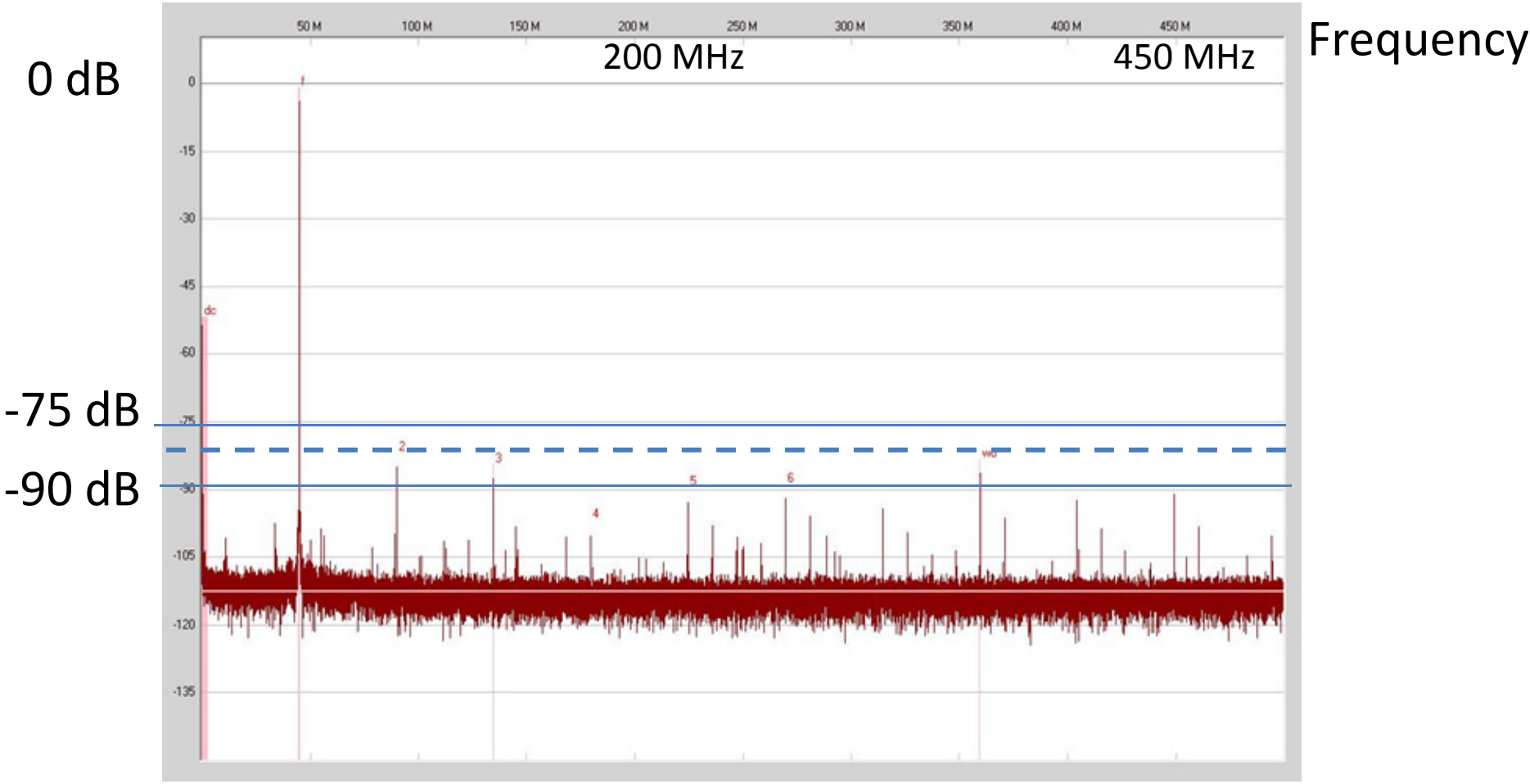


Frequency

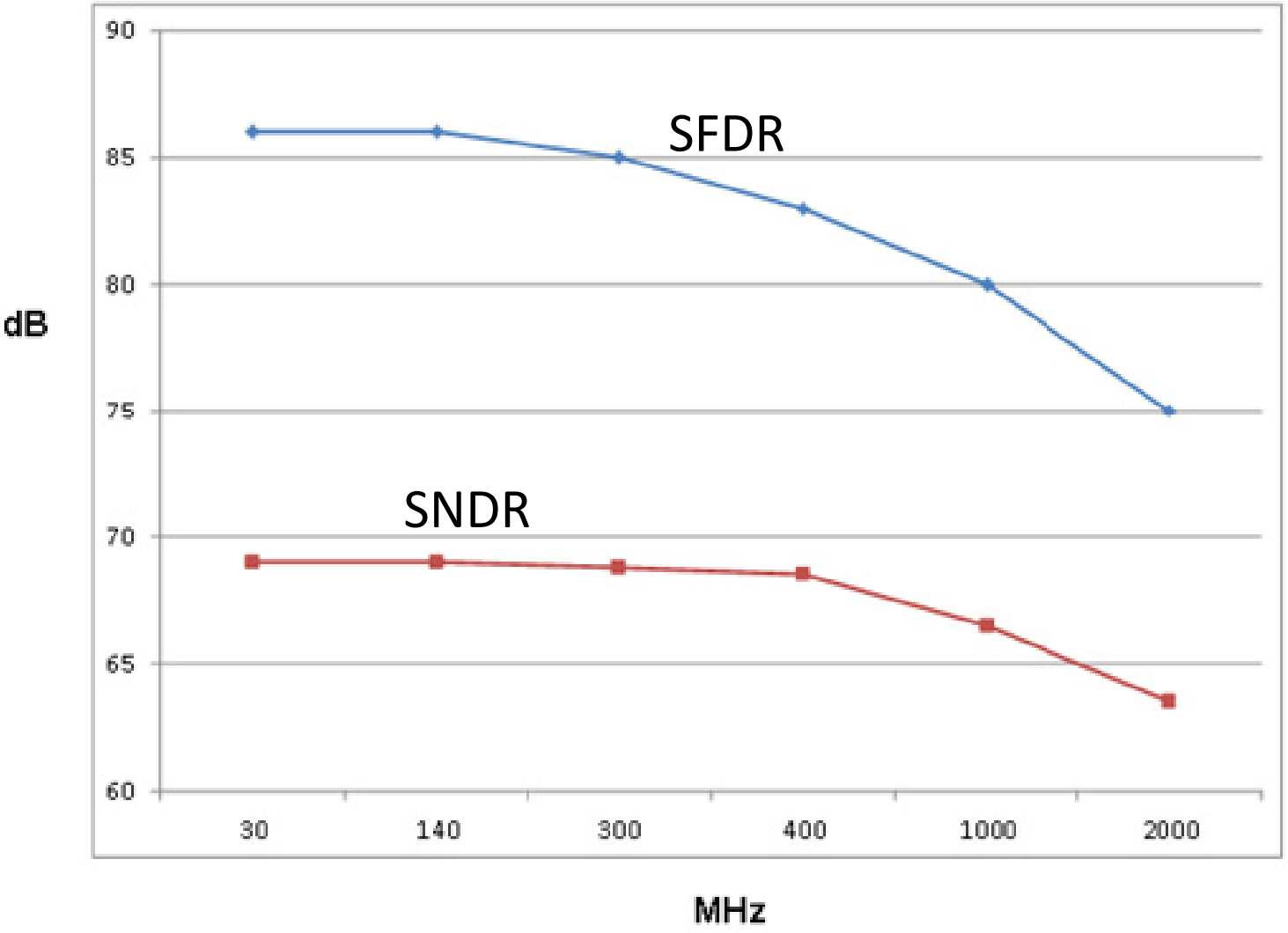
FFT at 1GS/s and Fin=800MHz
SFDR = 85dB at -1dBFS



FFT at 1GS/s and Fin=1.05GHz
SFDR = 82dB at -1dBFS



Performance with Input Frequency



Comparison to State-of-the-Art

	This Work	[R1]	[R2]	[R3]	[R4]	[R5]
Resolution	14b	14b	14b	12b	12b	12b
SNDR	69 dB	70 dB	61 dB	61 dB	58 dB	59 dB
SFDR	86 dB	86 dB	78 dB	74 dB	62 dB	67 dB
Noise Spectral Density (NSD)	156 dB/Hz	153 dB/Hz	152 dB/Hz	147.5 dB/Hz	149.8 dB/Hz	145 dB/Hz
Power	1.2 W	2.5 W	24 W	1.1 W	0.5 W	0.1 W
Sample Rate	1 GS/s	400 MS/s	2.5 GS/s	900 MS/s	3 GS/s	800 MS/s
FOM=SNDR+10log(BW/Power)	155.2 dB	149 dB	138 dB	147 dB	152.8 dB	154.8 dB
Interleaved	No	No	Yes	Yes	Yes	Yes

[R1] ADS5474, 14b 400MS/s ADC, Texas Instruments, http://www.ti.com.

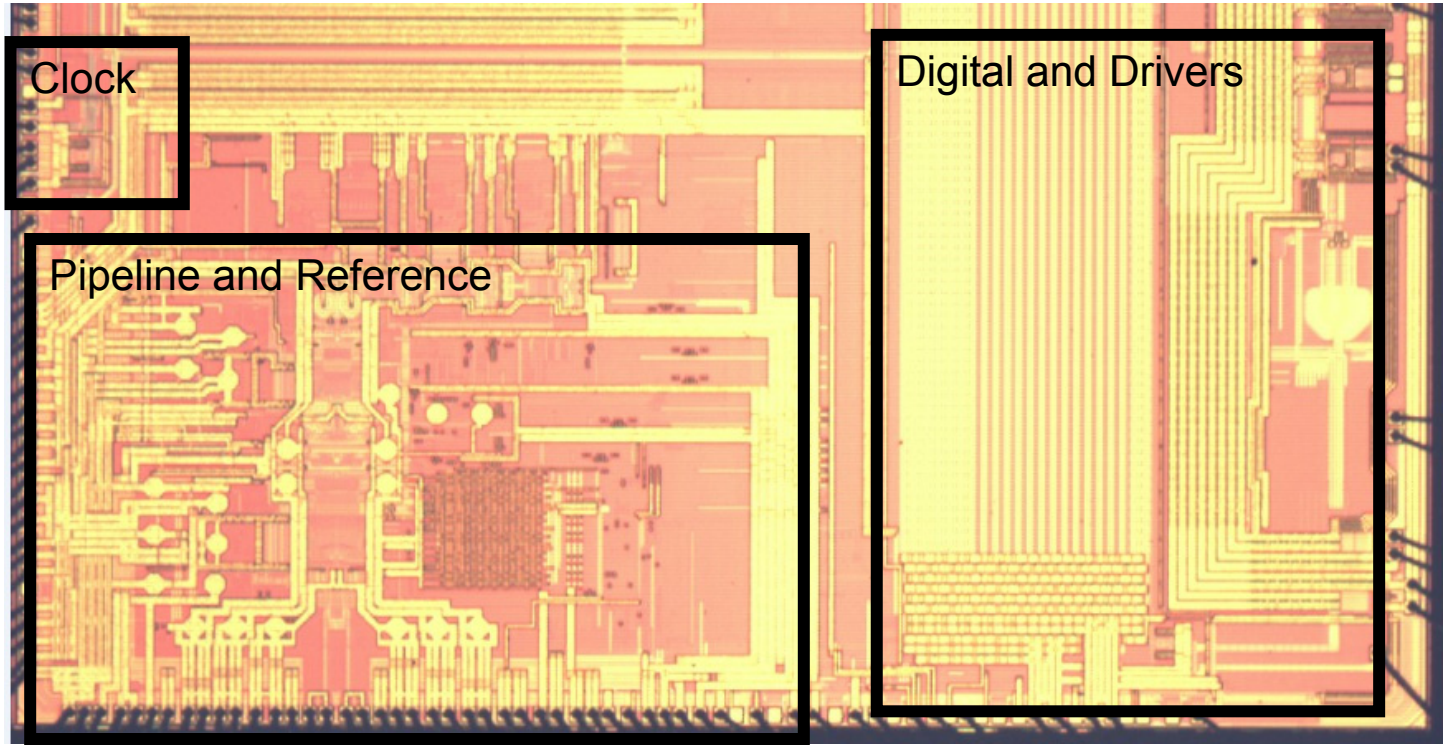
[R2] B. Setterberg, et al., "A 14b 2.5GS/s 8-Way-Interleaved Pipelined ADC with Background Calibration and Digital
Dynamic Linearity Correction", ISSCC Dig. Tech. Papers, pp. 466-468, Feb. 2013.

[R3] ADS5409, 12b 900MS/s ADC, Texas Instruments, http://www.ti.com.

[R4] C.-Y. Chen, et al., "A 12-Bit 3 GS/s Pipeline ADC With 0.4 mm and 500 mW in 40 nm Digital CMOS", J. Solid State Circuits, 47(4), pp. 1013-1021, April, 2012.

[R5] D. Vecchi, et al., "An 800 MS/s Dual-Residue Pipeline ADC in 40 nm CMOS", J. Solid State Circuits, 46(12), pp. 2834-2844, December, 2011.

Die Photo



Conclusion

- A 14b 1GS/s pipelined ADC is presented
- It employs analog circuit design techniques to improve performance and lower power consumption
- It employs background calibration to correct for inter-stage gain, memory, and input kick-back errors
- The background calibration shows robust performance with temperature, supply, sample rate, input amplitude and frequency

Acknowledgments

- Analog Devices HSC-ADC product line